# 1/2-Kbit I²C Serial EEPROM, Industrial Grade

## AT24C01C/AT24C02C

Product Page Links

## Features

- Low-Voltage Operation:
  - $V_{CC}$ = 1.7V to 5.5V
- Internally Organized as 128 x 8 (1K) or 256 x 8 (2K)
- Industrial Temperature Range: -40°C to +85°C
- I²C-Compatible (Two-Wire) Serial Interface:
  - 100 kHz Standard mode, 1.7V to 5.5V
  - 400 kHz Fast mode, 1.7V to 5.5V
  - 1 MHz Fast Mode Plus (FM+), 2.5V to 5.5V
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Write-Protect Pin for Full Array Hardware Data Protection
- Ultra Low Active Current (3 mA maximum) and Standby Current (6 µA maximum)
- 8-Byte Page Write Mode:
  - Partial page writes allowed
- Random and Sequential Read Modes
- Self-Timed Write Cycle Within 5 ms Maximum
- ESD Protection > 4,000V
- High Reliability:
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- RoHS Compliant
- Die Sale Options: Wafer Form and Bumped Wafers

## Packages

- 8-Lead PDIP, 8-Lead SOIC, 5-Lead SOT-23, 8-Lead TSSOP and 8-Pad UDFN


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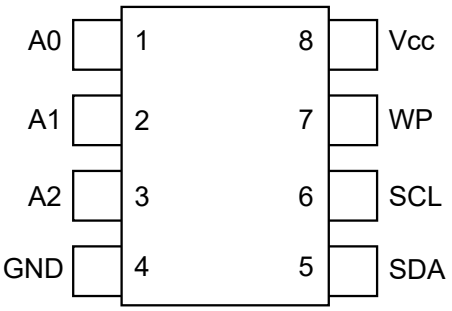
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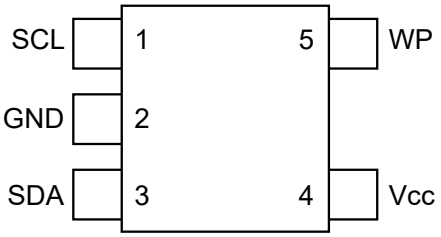

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# 1. Package Types (not to scale)

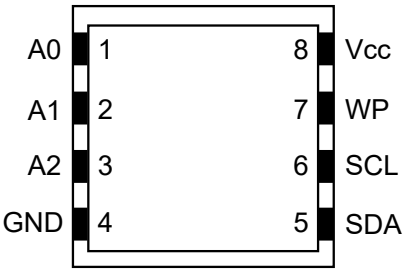
**8-Lead PDIP/SOIC/TSSOP**
(Top View)




**5-Lead SOT-23**
(Top View)




**8-Pad UDFN**
(Top View)




**Note:**

1. Refer to Device Addressing for details about addressing the SOT-23 version of the device.


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# 2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

**Table 2-1.** Pin Function Table

| Name | 8-Lead PDIP | 8-Lead SOIC | 8-Lead TSSOP | 5-Lead SOT-23 | 8-Pad UDFN(1) | Function |
|---|---|---|---|---|---|---|
| A0(2) | 1 | 1 | 1 | — | 1 | Device Address Input |
| A1(2) | 2 | 2 | 2 | — | 2 | Device Address Input |
| A2(2) | 3 | 3 | 3 | — | 3 | Device Address Input |
| GND | 4 | 4 | 4 | 2 | 4 | Ground |
| SDA | 5 | 5 | 5 | 3 | 5 | Serial Data |
| SCL | 6 | 6 | 6 | 1 | 6 | Serial Clock |
| WP(2) | 7 | 7 | 7 | 5 | 7 | Write-Protect |
| $V_{CC}$ | 8 | 8 | 8 | 4 | 8 | Device Power Supply |

**Notes:**

1. The exposed pad on this package can be connected to GND or left floating.
2. If the A0, A1, A2 or WP pins are not driven, they are internally pulled down to GND. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once these pins are biased above the CMOS input buffer's trip point (~0.5 x $V_{CC}$), the pull-down mechanism disengages. Microchip recommends connecting these pins to a known state whenever possible.

## 2.1. Device Address Inputs (A0, A1, A2)

The A0, A1 and A2 pins serve as device address inputs and are typically hardwired directly to either GND or $V_{CC}$ to maintain compatibility with other Two-Wire Serial EEPROM devices. By configuring these pins appropriately, up to eight devices can coexist on a single bus system. A device is selected only when both the hardware address and software address match. If the A0, A1 and A2 pins are left floating, they are internally pulled down to GND. However, capacitive coupling in certain applications may cause unintended behavior. To ensure reliable operation, Microchip recommends connecting all address pins to a defined logic level. When pull-up resistors are used, a resistance value of 10 kΩ or lower is recommended.

## 2.2. Ground

The ground reference for the power supply. GND should be connected to the system ground.

## 2.3. Serial Data (SDA)

The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled high using an external pull-up resistor (not to exceed 10 kΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.

## 2.4. Serial Clock (SCL)

The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin are always latched in on the rising edge of SCL, while output data on the SDA pin are clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled high using an external pull-up resistor.

## 2.5. Write-Protect (WP)

When the write-protect (WP) input is connected to GND, normal write operations are enabled. When the WP pin is connected directly to $V_{CC}$, all write operations to the protected memory area are disabled.

If the WP pin is left floating, it is internally pulled down to GND. However, because capacitive coupling may occur in customer applications, Microchip recommends connecting the WP pin to


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a defined logic level at all times. When a pull-up resistor is used, a value of 10 kΩ or less is recommended.

**Table 2-2.** Write-Protect

| WP Pin Status | Protected Memory Area |
|---|---|
| At $V_{CC}$ | Full Array |
| At GND | Normal Write Operations |

## 2.6. Device Power Supply

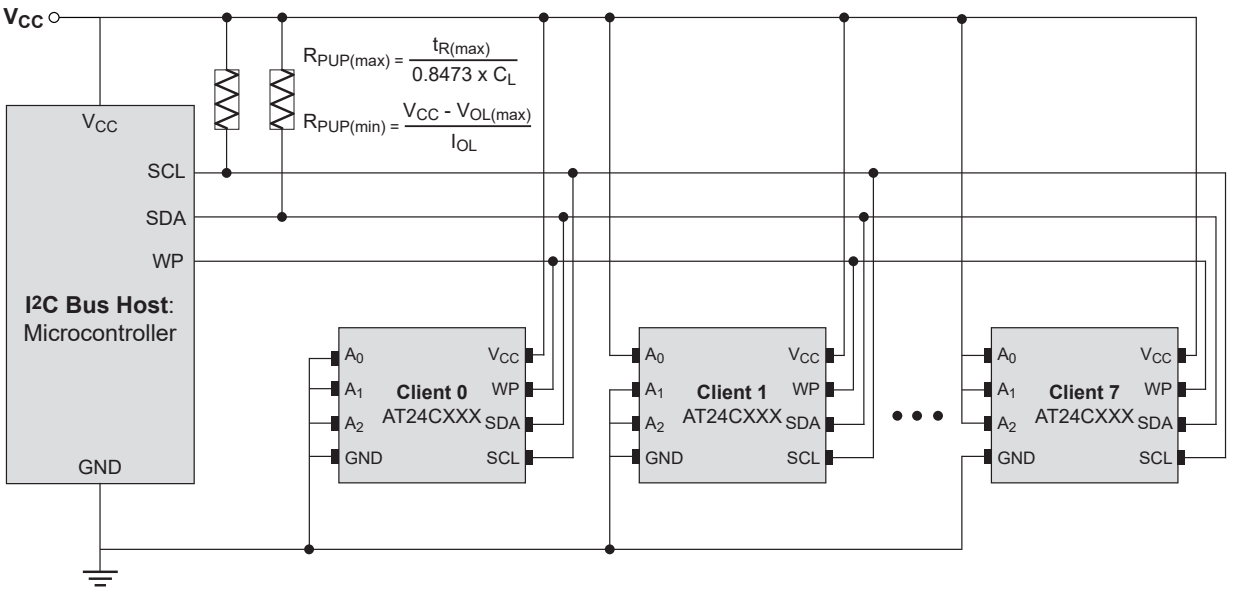
The $V_{CC}$ pin is used to supply the source voltage to the device. Operations at invalid $V_{CC}$ voltages may produce spurious results and should not be attempted.


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# 3. Description

The AT24C01C/AT24C02C provides 1,024/2,048 bits of Serial Electrically Erasable Programmable Read-Only Memory (EEPROM) organized as 128/256 words of 8 bits each. The device's cascading feature allows up to eight devices to share a common Two-Wire bus. This device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The device is available in space-saving 8-Lead PDIP, 8-Lead SOIC, 5-Lead SOT-23, 8-Lead TSSOP and 8-Pad UDFN packages. All packages operate from 1.7 to 5.5V.

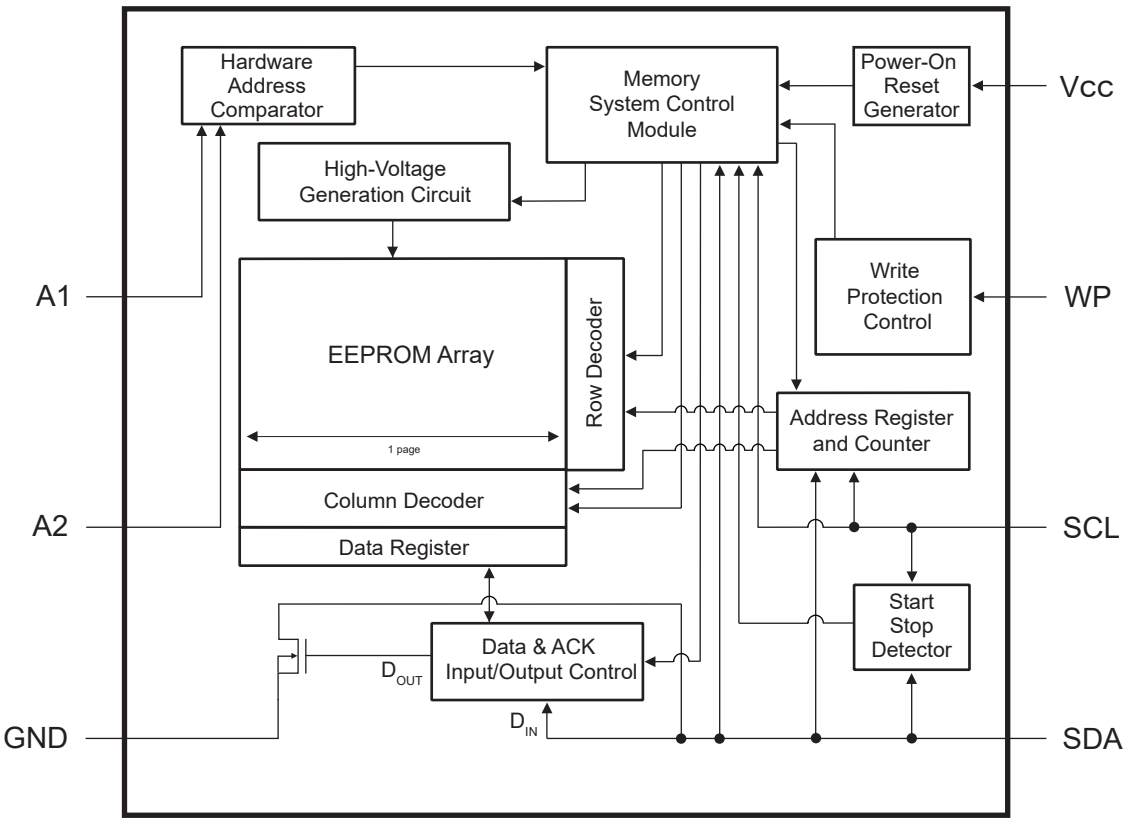
## 3.1. System Configuration Using Two-Wire Serial EEPROMs





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## 3.2. Block Diagram





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# 4. Electrical Characteristics

## 4.1. Absolute Maximum Ratings

| | |
|---|---|
| **Temperature under bias** | -55°C to +125°C |
| **Storage temperature** | -65°C to +150°C |
| **$V_{CC}$** | 6.25V |
| **Voltage on any pin with respect to ground** | -1.0V to +7.0V |
| **DC output current** | 5.0 mA |
| **ESD protection** | > 4 kV |

**Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 4.2. DC and AC Operating Range

**Table 4-1.** DC and AC Operating Range

| AT24C01C/AT24C02C | | |
|---|---|---|
| Operating Temperature (Case) | Industrial Temperature Range | -40°C to +85°C |
| $V_{CC}$ Power Supply | Low-Voltage Grade | 1.7V to 5.5V |

## 4.3. DC Characteristics

**Table 4-2.** DC Characteristics

| Parameter | Symbol | Min. | Typ.(1) | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 1.7 | — | 5.5 | V | |
| Supply Current | $I_{CC1}$ | — | 0.4 | 1.0 | mA | $V_{CC}$ = 5.0V, Read at 400 kHz |
| Supply Current | $I_{CC2}$ | — | 2.0 | 3.0 | mA | $V_{CC}$ = 5.0V, Write at 400 kHz |
| Standby Current | $I_{SB}$ | — | — | 1.0 | µA | $V_{CC}$ = 1.7V, $V_{IN}$ = $V_{CC}$ or GND |
| | | — | — | 2.0 | µA | $V_{CC}$ = 2.5V, $V_{IN}$ = $V_{CC}$ or GND |
| | | — | — | 6.0 | µA | $V_{CC}$ = 5.5V, $V_{IN}$ = $V_{CC}$ or GND |
| Input Leakage Current | $I_{LI}$ | — | 0.10 | 3.0 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| Output Leakage Current | $I_{LO}$ | — | 0.05 | 3.0 | µA | $V_{OUT}$ = $V_{CC}$ or GND |
| Input Low Level | $V_{IL}$ | -0.6 | — | $V_{CC}$ x 0.3 | V | Note 2 |
| Input High Level | $V_{IH}$ | $V_{CC}$ x 0.7 | — | $V_{CC}$ + 0.5 | V | Note 2 |
| Output Low Level | $V_{OL1}$ | — | — | 0.2 | V | $V_{CC}$ = 1.7V, $I_{OL}$ = 0.15 mA |
| Output Low Level | $V_{OL2}$ | — | — | 0.4 | V | $V_{CC}$ = 3.0V, $I_{OL}$ = 2.1 mA |

**Note:**

1. Typical values characterized at $T_A$ = +25°C unless otherwise noted.
2. This parameter is characterized but is not 100% tested in production.


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## 4.4. AC Characteristics

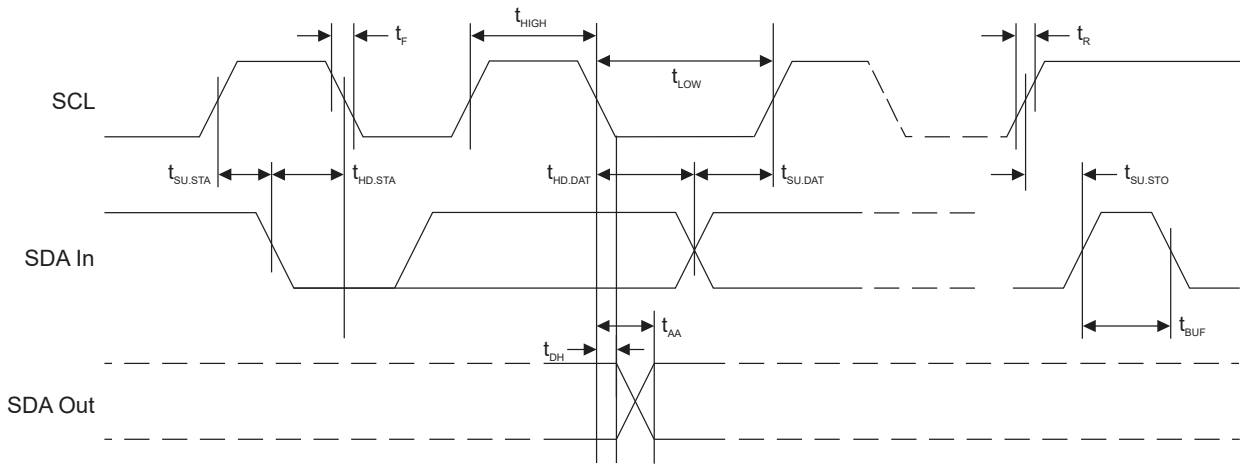
**Table 4-3.** AC Characteristics[1]

| Parameter | Symbol | Fast Mode | | Fast Mode Plus | | Units |
|---|---|---|---|---|---|---|
| | | $V_{CC}$ = 1.7V to 5.5V | | $V_{CC}$ = 2.5V to 5.5V | | |
| | | Min. | Max. | Min. | Max. | |
| Clock Frequency, SCL | $f_{SCL}$ | — | 400 | — | 1000 | kHz |
| Clock Pulse Width Low | $t_{LOW}$ | 1,200 | — | 500 | — | ns |
| Clock Pulse Width High | $t_{HIGH}$ | 600 | — | 400 | — | ns |
| Input Filter Spike Suppression | $t_I$ | — | 100 | — | 50 | ns |
| Clock Low to Data Out Valid | $t_{AA}$ | 100 | 900 | 50 | 450 | ns |
| Bus Free Time between Stop and Start | $t_{BUF}$ | 1,200 | — | 500 | — | ns |
| Start Hold Time | $t_{HD.STA}$ | 600 | — | 250 | — | ns |
| Start Set-Up Time | $t_{SU.STA}$ | 600 | — | 250 | — | ns |
| Data In Hold Time | $t_{HD.DAT}$ | 0 | — | 0 | — | ns |
| Data In Set-up Time | $t_{SU.DAT}$ | 100 | — | 100 | — | ns |
| Inputs Rise Time[2] | $t_R$ | — | 300 | — | 300 | ns |
| Inputs Fall Time[2] | $t_F$ | — | 300 | — | 100 | ns |
| Stop Set-Up Time | $t_{SU.STO}$ | 600 | — | 250 | — | ns |
| Data Out Hold Time | $t_{DH}$ | 50 | — | 50 | — | ns |
| Write Cycle Time | $t_{WR}$ | — | 5 | — | 5 | ms |

**Notes:**

1. AC measurement conditions:
   - $C_L$: 100 pF
   - $R_{PUP}$ (SDA bus line pull-up resistor to $V_{CC}$): 1.3 kΩ (1000 kHz), 4 kΩ (400 kHz), 10 kΩ (100 kHz)
   - Input pulse voltages: 0.3 x $V_{CC}$ to 0.7 x $V_{CC}$
   - Input rise and fall times: ≤ 50 ns
   - Input and output timing reference voltages: 0.5 x $V_{CC}$
2. These parameters are determined through product characterization and are not 100% tested in production.

**Figure 4-1.** Bus Timing





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## 4.5. Electrical Specifications

### 4.5.1. Power-Up Requirements and Reset Behavior

During a power-up sequence, the $V_{CC}$ supplied to the AT24C01C/AT24C02C should monotonically rise from GND to the minimum $V_{CC}$ level (as specified in Table 4-1), with a slew rate no faster than 0.1 V/µs.

#### 4.5.1.1. Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT24C01C/AT24C02C includes a Power-On Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the $V_{CC}$ level crosses the internal voltage threshold ($V_{POR}$) that brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the $V_{CC}$ supply has reached a stable value greater than or equal to the minimum $V_{CC}$ level. Additionally, once the $V_{CC}$ is greater than or equal to the minimum $V_{CC}$ level, the bus host must wait at least $t_{PUP}$ before sending the first command to the device. See Table 4-4 for the values associated with these power-up parameters.

**Table 4-4.** Power-Up Conditions[1]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{PUP}$ | Time required after $V_{CC}$ is stable before the device can accept commands | 100 | — | µs |
| $V_{POR}$ | Power-On Reset Threshold Voltage | — | 1.5 | V |
| $t_{POFF}$ | Minimum time at $V_{CC}$ = 0V between power cycles | 500 | — | ms |

**Note:**

1. These parameters are characterized but they are not 100% tested in production.

If an event occurs in the system where the $V_{CC}$ level supplied to the AT24C01C/AT24C02C drops below the maximum $V_{POR}$ level specified, it is recommended that a full power cycle sequence be performed by first driving the $V_{CC}$ pin to GND, waiting at least the minimum $t_{POFF}$ time and then performing a new power-up sequence in compliance with the requirements defined in this section.

### 4.5.2. Pin Capacitance

**Table 4-5.** Pin Capacitance[1]

| Symbol | Test Condition | Max. | Units | Conditions |
|---|---|---|---|---|
| $C_{I/O}$ | Input/Output Capacitance (SDA) | 8 | pF | $V_{I/O}$ = 0V |
| $C_{IN}$ | Input Capacitance (A0, A1, A2 and SCL) | 6 | pF | $V_{IN}$ = 0V |

**Note:**

1. This parameter is characterized but is not 100% tested in production.

### 4.5.3. EEPROM Cell Performance Characteristics

**Table 4-6.** EEPROM Cell Performance Characteristics

| Operation | Test Condition | Min. | Max. | Units |
|---|---|---|---|---|
| Write Endurance[1] | $T_A$ = +25°C, $V_{CC}$ = 3.3V, Page Write mode | 1,000,000 | — | Write Cycles |
| Data Retention[1] | $T_A$ = +55°C | 100 | — | Years |

**Note:**

1. Performance is determined through characterization and the qualification process.


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# 5. Device Operation and Communication

The AT24C01C/AT24C02C operates as a client device and utilizes a simple $I^2C$-compatible Two-Wire digital serial interface to communicate with a host controller, commonly referred to as the bus host. The host initiates and controls all read and write operations to the client devices on the serial bus, and both the host and the client devices can transmit and receive data on the bus.

The serial interface consists of two signal lines: Serial Clock (SCL) and Serial Data (SDA).
The SCL pin is used to receive the clock signal from the host, while the bidirectional SDA pin is used to receive command and data information from the host as well as to send data back to the host. Data are always latched into the AT24C01C/AT24C02C on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pins incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most Significant bit (MSb) first. During bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data have been transferred, the receiving device must respond with either an Acknowledge (ACK) or a No-Acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the host. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any read or write operation; thus, there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must change only while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and terminate all serial bus communication between the host and the client devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the host. For the serial bus to be idle, both the SCL and SDA pins must be in the logic high state simultaneously.

## 5.1. Clock and Data Transition Requirements

The SDA pin is an open-drain terminal and therefore must be pulled high with an external pull-up resistor. SCL is an input pin that can either be driven high or pulled high using an external pull-up resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below. The relationship of the AC timing parameters with respect to SCL and SDA for the AT24C01C/AT24C02C is shown in the timing waveform in Figure 4-1. The AC timing characteristics and specifications are outlined in AC Characteristics.

## 5.2. Start and Stop Conditions

### 5.2.1. Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is at a stable logic '1' state, which will bring the device out of Standby mode. The host initiates any data transfer sequence with a Start condition; thus, every command must commence with this condition. The device continuously monitors the SDA and SCL pins for a Start condition and will only respond when one is detected. Refer to Figure 5-1 for more details.

### 5.2.2. Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the logic '1' state.

The host can use the Stop condition to end a data transfer sequence with the AT24C01C/AT24C02C, which will subsequently return to Standby mode. The host can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the host will perform another operation. Refer to Figure 5-1 for more details.


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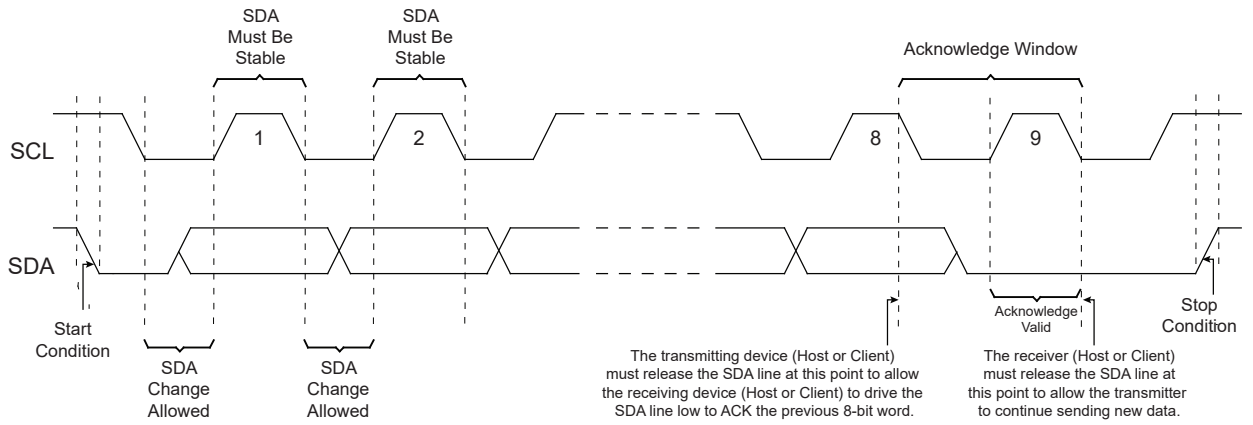
## 5.3. Acknowledge and No-Acknowledge

After each byte of data is received, the receiving device must confirm with the transmitting device that it has successfully received the data byte by responding with an Acknowledge (ACK). An ACK occurs when the transmitting device releases the SDA line at the falling edge of the eighth clock cycle, followed by the receiving device responding with a logic '0' throughout the ninth clock cycle's high period.

When the AT24C01C/AT24C02C transmits data to the host, the host can indicate that it has finished receiving data and wants to end the operation by sending a logic '1' response to the AT24C01C/AT24C02C instead of an ACK response during the ninth clock cycle. This is known as a No-Acknowledge (NACK) and is accomplished when the host sends a logic '1' during the ninth clock cycle, at which point the AT24C01C/AT24C02C will release the SDA line so the host can then generate a Stop condition.

The transmitting device, which can be either the bus host or the Serial EEPROM, must release the SDA line at the falling edge of the eighth clock cycle to allow the receiving device to drive the SDA line to a logic '0' to ACK the previous 8-bit word. The receiving device must release the SDA line at the end of the ninth clock cycle to allow the transmitter to continue sending new data. A timing diagram is provided in Figure 5-1 to better illustrate these requirements.

**Figure 5-1.** Start Condition, Data Transitions, Stop Condition and Acknowledge




## 5.4. Standby Mode

The AT24C01C/AT24C02C features a low-power Standby mode that is enabled when any one of the following occurs:

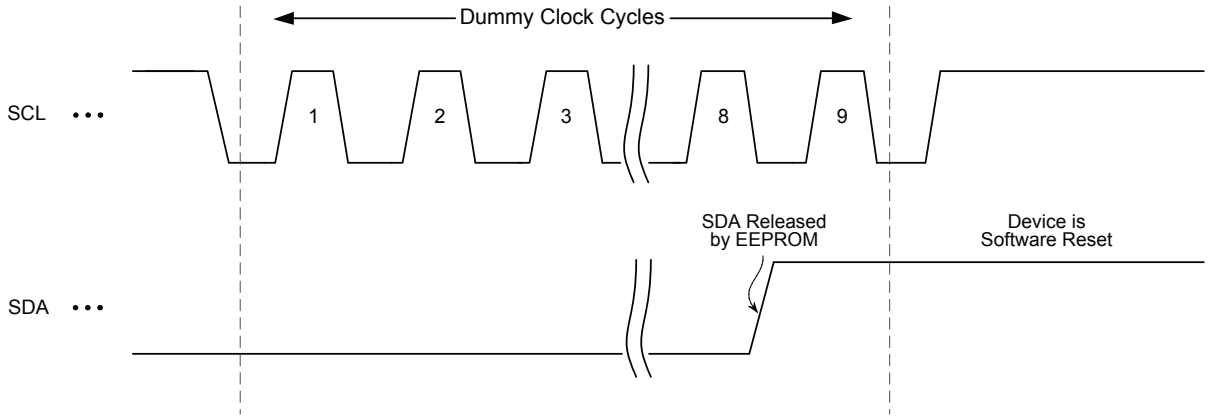
- A valid power-up sequence is performed (see Power-Up Requirements and Reset Behavior).
- A Stop condition at the end of a valid $I^2C$ transaction is received by the device unless it initiates an internal write cycle (see Write Operations).
- At the completion of an internal write cycle (see Write Operations).

## 5.5. Software Reset

After an interruption in protocol, power loss or system Reset, any Two-Wire device can be protocol reset by clocking SCL until SDA is released by the EEPROM and goes high. The number of clock cycles until SDA is released by the EEPROM will vary. The software Reset sequence should not take more than nine dummy clock cycles. Once the software Reset sequence is complete, a new protocol can be sent to the device by sending a Start condition followed by the protocol. Refer to Figure 5-2 for an illustration.


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**Figure 5-2.** Software Reset




In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device (see Power-Up Requirements and Reset Behavior).


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# 6. Memory Organization

The AT24C01C is internally organized as 16 pages of 8 bytes each. The AT24C02C is internally organized as 32 pages of 8 bytes each.

## 6.1. Device Addressing

Accessing the device requires an 8-bit device address byte following a Start condition to enable the device for a read or write operation. Since multiple client devices can reside on the serial bus, each client device must have its own unique address so the host can access each device independently.

The Most Significant four bits of the device address byte is referred to as the device type identifier. The device type identifier '1010' (Ah) is required in bits 7 through 4 of the device address byte (see Table 6-1).

Following the 4-bit device type identifier are the hardware client address bits, A2, A1 and A0. These bits can be used to expand the address space by allowing up to eight Serial EEPROM devices on the same bus. These hardware client address bits must correlate with the voltage level on the corresponding hardwired device address input pins A0, A1 and A2. The A0, A1 and A2 pins use an internal proprietary circuit that automatically biases the pin to a logic '0' state if the pin is allowed to float. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once the pin is biased above the CMOS input buffer's trip point (~0.5 x $V_{CC}$), the pull-down mechanism disengages. Microchip recommends connecting the A0, A1 and A2 pins to a known state whenever possible.

When using the SOT-23 package, the A2, A1 and A0 pins are not accessible and are left floating. The previously mentioned automatic pull-down circuit will set this pin to a logic '0' state. As a result, to properly communicate with the device in the SOT-23 package, the A2, A1 and A0 software bits must always be set to logic '0' for any operation. Refer to Table 6-1 to review these bit positions.

The eighth bit (bit 0) of the device address byte is the Read/Write Select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon the successful comparison of the device address byte, the AT24C01C/AT24C02C will return an ACK. If a valid comparison is not made, the device will NACK.

**Table 6-1.** Device Address Byte

| Package | Device Type Identifier | | | | Hardware Client Address Bits | | | R/$\overline{W}$ Select |
|---|---|---|---|---|---|---|---|---|
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| PDIP, SOIC, TSSOP, UDFN | 1 | 0 | 1 | 0 | A2 | A1 | A0 | R/$\overline{W}$ |
| SOT-23 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ |

For all operations except the current address read, a word address byte must be transmitted to the device immediately following the device address byte. The word address byte contains a 7-bit (in the case of the AT24C01C) or 8-bit (in the case of the AT24C02C) memory array word address, and is used to specify which byte location in the EEPROM to start reading or writing. Refer to Table 6-2 to review these bit positions.

**Table 6-2.** Word Address Byte

| Device | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| AT24C01C | X[1] | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| AT24C02C | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

**Note:**

1. Bit 7 is a "don't care" bit on the AT24C01C.


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# 7. Write Operations

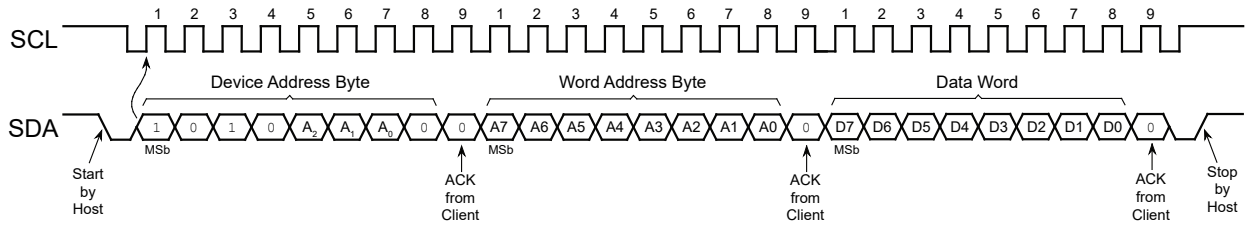
All write operations for the AT24C01C/AT24C02C begin with the host sending a Start condition, followed by a device address byte with the R/$\overline{W}$ bit set to logic '0', and then by the word address byte. The data value(s) to be written to the device immediately follow the word address byte.

## 7.1. Byte Write

The AT24C01C/AT24C02C supports the writing of a single 8-bit byte. Selecting a data word in the AT24C01C requires a 7-bit word address, while selecting a data word in the AT24C02C requires an 8-bit word address.

Upon receipt of the proper device address and the word address bytes, the EEPROM will send an Acknowledge. The device will then be ready to receive the 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will respond with an ACK. The addressing device, such as a bus host, must then terminate the write operation with a Stop condition. At that time, the EEPROM will enter an internally self-timed write cycle, which will be completed within $t_{WR}$, while the data word is being programmed into the nonvolatile EEPROM. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete.

**Figure 7-1.** Byte Write




## 7.2. Page Write

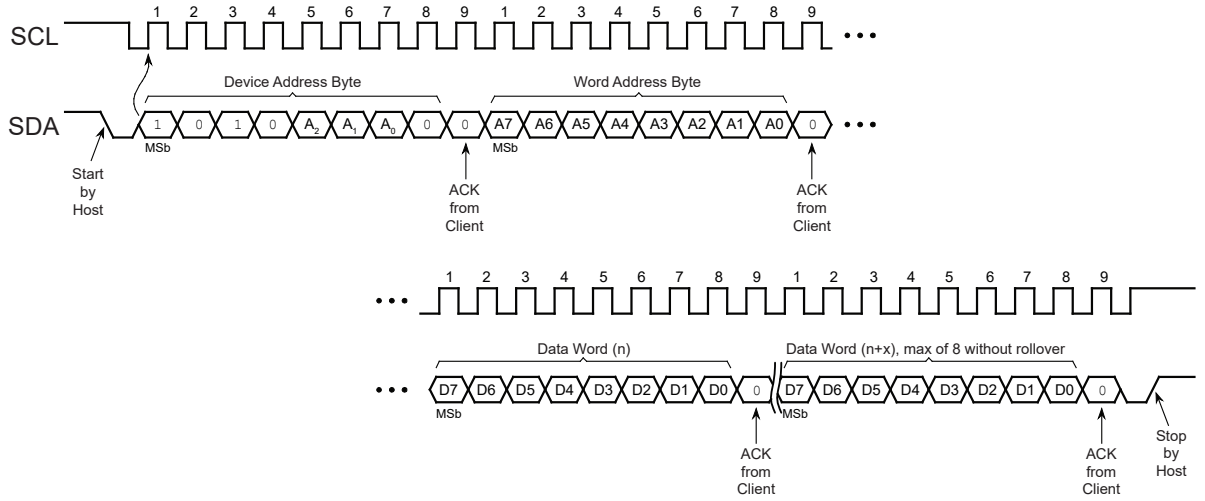
A page write operation allows up to 8 bytes to be written in a single write cycle, provided that all bytes are in the same row of the memory array (where address bits A7 to A3 are identical). Partial page writes of fewer than 8 bytes are also allowed.

A page write is initiated the same way as a byte write, but the bus host does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the bus host can transmit up to seven additional data words. The EEPROM will respond with an ACK after each data word is received. Once all data to be written have been sent to the device, the bus host must issue a Stop condition (see Figure 7-2), at which point the internally self-timed write cycle will begin.

The lower three bits of the word address are internally incremented following the receipt of each data word. The higher-order address bits are not incremented and retain the memory page row location. Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes being written. When the incremented word address reaches the page boundary, the address counter will roll over to the beginning of the same page. Nevertheless, creating a rollover event should be avoided as previously loaded data in the page could become unintentionally altered.


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**Figure 7-2.** Page Write

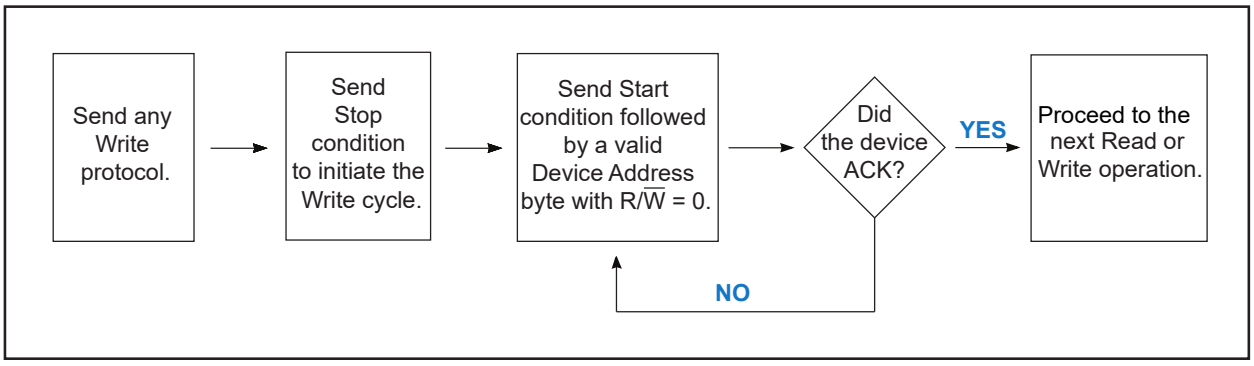



## 7.3. Acknowledge Polling

An Acknowledge Polling routine can be implemented to optimize time-sensitive applications that aim to avoid waiting for the fixed maximum write cycle time ($t_{WR}$). This method allows the application to promptly determine when the Serial EEPROM write cycle has completed so a subsequent operation can be started.

Once the internally self-timed write cycle has started, an Acknowledge Polling routine can be initiated. This involves repeatedly sending a Start condition followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '0'. The device will not respond with an ACK while the write cycle is ongoing. Once the internal write cycle has completed, the EEPROM will respond with an ACK, allowing a new read or write operation to be immediately initiated. A flowchart has been included in Figure 7-3 to better illustrate this technique.

**Figure 7-3.** Acknowledge Polling Flowchart

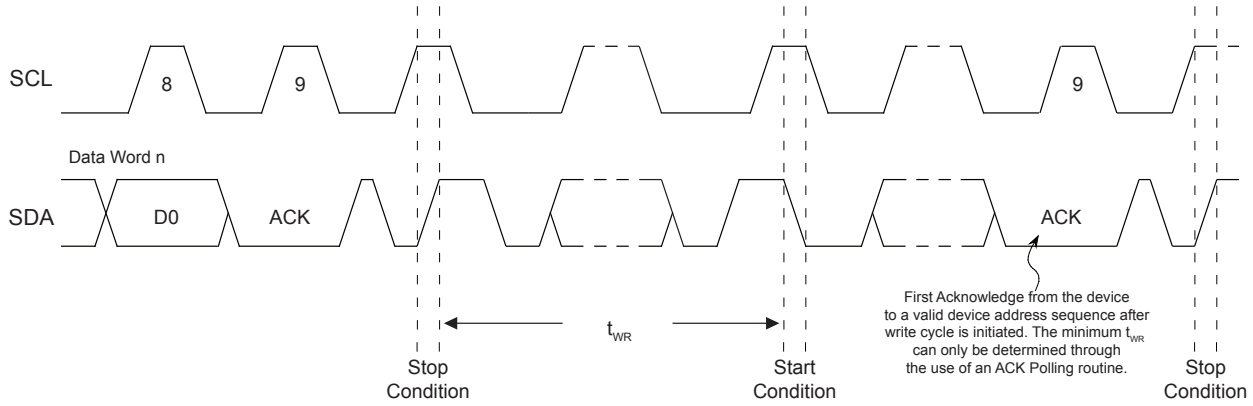



## 7.4. Write Cycle Timing

The length of the self-timed write cycle ($t_{WR}$) is defined as the amount of time from the Stop condition, which begins the internal write cycle, to the Start condition of the first device address byte sent to the AT24C01C/AT24C02C, to which it subsequently responds with an ACK. Figure 7-4 shows this measurement. During the internally self-timed write cycle, any attempts to read from or write to the memory array will not be processed.


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**Figure 7-4.** Write Cycle Timing




## 7.5. Write Protection

The AT24C01C/AT24C02C utilizes a hardware data protection scheme that allows the user to write-protect the entire memory contents when the WP pin is at $V_{CC}$ (or a valid $V_{IH}$). No write protection will be set if the WP pin is at GND or left floating.

**Table 7-1.** AT24C01C/AT24C02C Write-Protect Behavior

| WP Pin Voltage | Part of the Array Protected |
|---|---|
| $V_{CC}$ | Full Array |
| GND | None — Write Protection Not Enabled |

The status of the WP pin is sampled at the Stop condition for every byte write or page write operation prior to the start of an internally self-timed write cycle. Changing the WP pin state after the Stop condition has been sent will not alter or interrupt the execution of the write cycle.

If an attempt is made to write to the device while the WP pin has been asserted, the device will acknowledge the device address, word address and data bytes, but no write cycle will occur when the Stop condition is issued. The device will immediately be ready to accept a new read or write command.


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# 8. Read Operations

Read operations are initiated in the same way as write operations, with the exception that the Read/Write Select bit in the device address byte must be a logic '1'. There are three read operations:

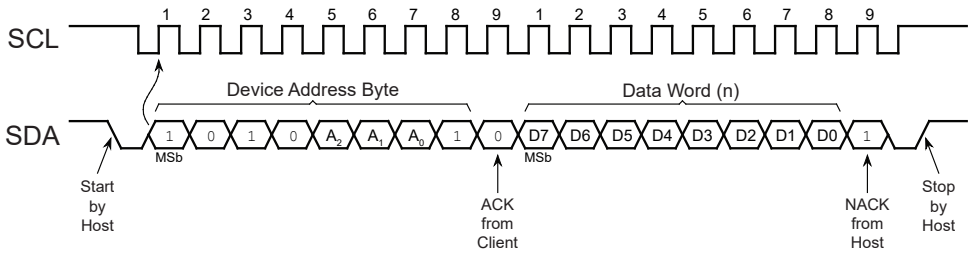
- Current Address Read
- Random Read
- Sequential Read

## 8.1. Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the $V_{CC}$ is maintained to the part. The address rollover during a read is from the last byte of the last page to the first byte of the first page of the memory.

A current address read operation will output data according to the location of the internal data word address counter. This is initiated with a Start condition, followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '1'. The device will ACK this sequence and the current address data word is serially clocked out on the SDA line. All types of read operations will be terminated if the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

**Figure 8-1.** Current Address Read

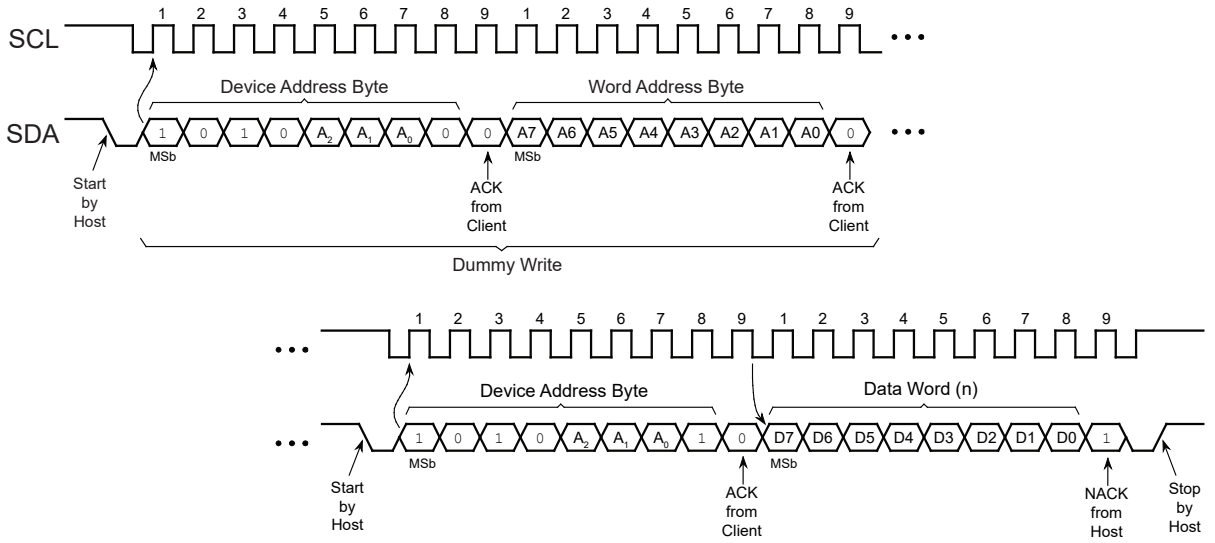



## 8.2. Random Read

A random read begins in the same way as a byte write operation does to load a new data word address. This is known as a "dummy write" sequence; however, the data byte and the Stop condition of the byte write must be omitted to prevent the part from entering an internal write cycle. Once the device address and word address are clocked in and acknowledged by the EEPROM, the bus host must generate another Start condition. The bus host then initiates a current address read by sending a Start condition, followed by a valid device address byte with the R/W bit set to logic '1'.

The EEPROM will ACK the device address and serially clock out the data word on the SDA line. All types of read operations will be terminated if the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

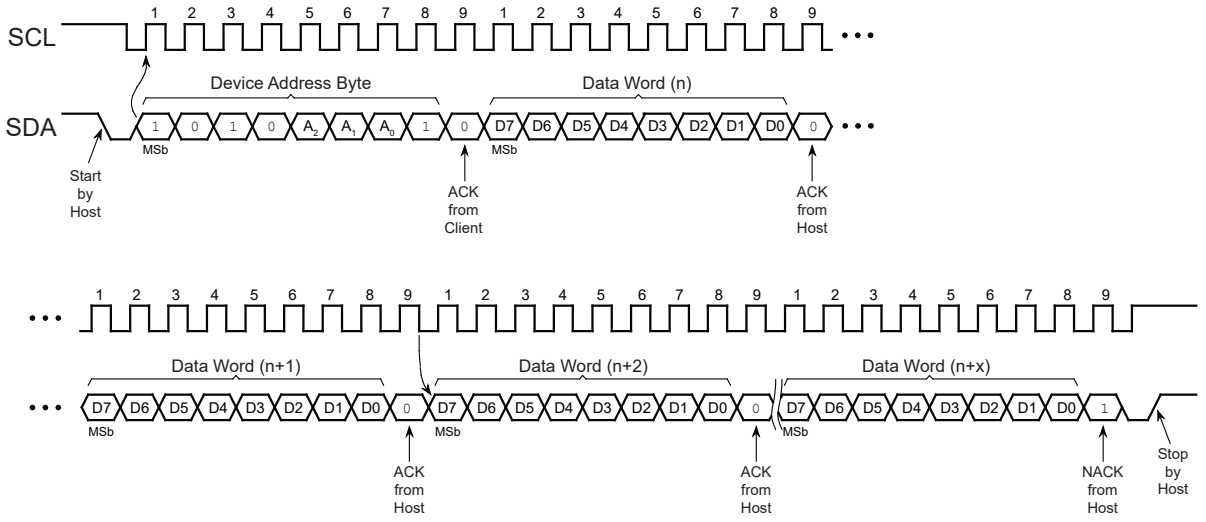

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## 8.3. Sequential Read

Sequential Reads are initiated through either a Current Address Read or a Random Read, as described previously. As long as the EEPROM receives an ACK, it continues incrementing the word address and serially clocking out sequential data words. When the maximum memory address is reached, the address rolls over, and the sequential read continues from the beginning of the memory array. All read operations are terminated if the bus host does not respond with an ACK (that is, it issues a NACK) during the ninth clock cycle. Following the NACK response, the host may issue a Stop condition to complete the protocol or issue a Start condition to begin the next sequence.

**Figure 8-2.** Sequential Read





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# 9. Device Default Condition from Microchip

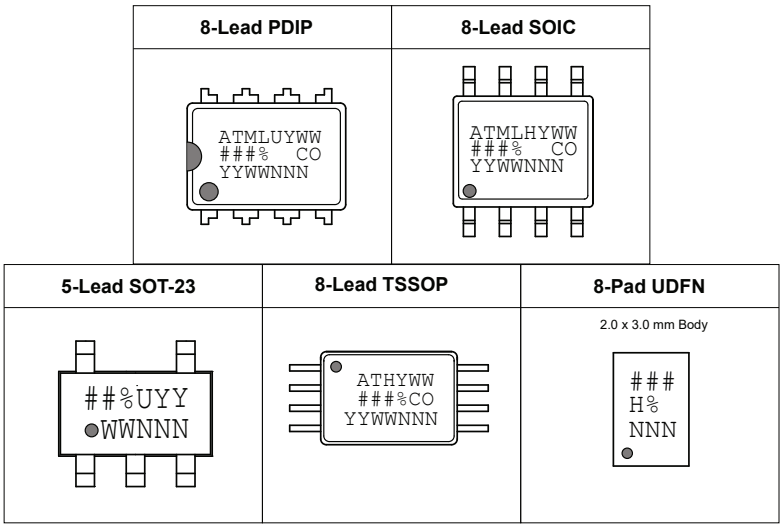
The AT24C01C/AT24C02C is delivered with the EEPROM array set to logic '1', resulting in FFh data in all locations.


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# 10. Packaging Information

## 10.1. Package Marking Information

### AT24C01C and AT24C02C: Package Marking Information




**Note:** ● designates pin 1
**Note 2:** Package drawings are not to scale
**Note 3:** For SOT-23 package with date codes before 7B, the bottom line (YMXX) is marked on the bottom side and there is no Country of Assembly (@) mark on the top line.

| **Catalog Number Truncation** | |
|---|---|
| AT24C01C | Truncation Code ###: 01C / ##: 1C |
| AT24C02C | Truncation Code ###: 02C / ##: 2C |

| **Date Codes** | **Voltages** |
|---|---|
| Y = Year code (last digit of calendar year)<br>YY = Year code (last 2 digits of calendar year)<br>WW = Week code (week of January 1 is week '01') | % = Minimum Voltage<br>M: 1.7V min |

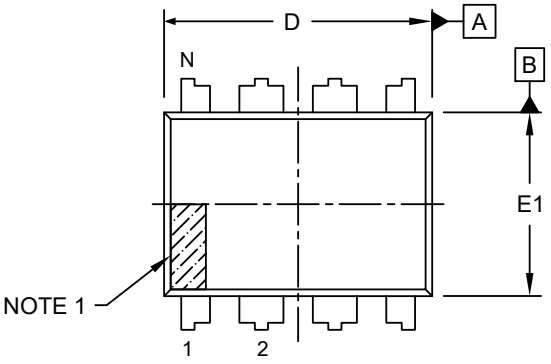
| **Country of Origin** | **Device Grade** | **Atmel Truncation** |
|---|---|---|
| CO = Country of Origin | H or U: Industrial Grade | AT: Atmel<br>ATM: Atmel<br>ATML: Atmel |

| **Trace Code** |
|---|
| NNN = Alphanumeric Trace Code (2 Characters for Small Package) |

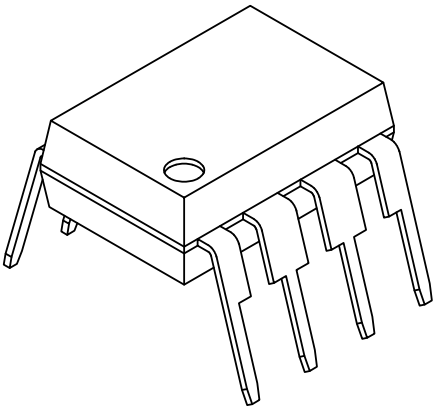

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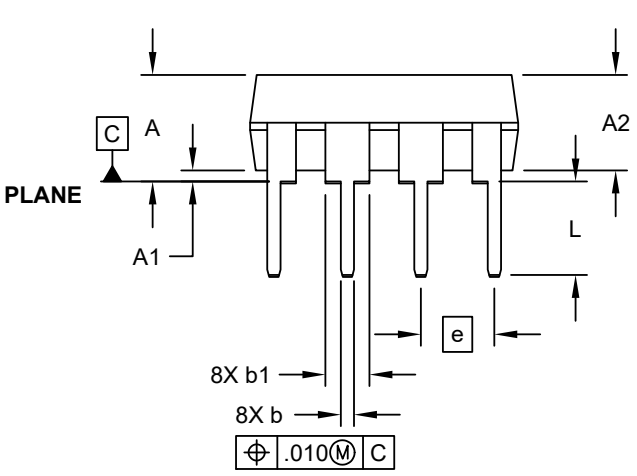
## 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

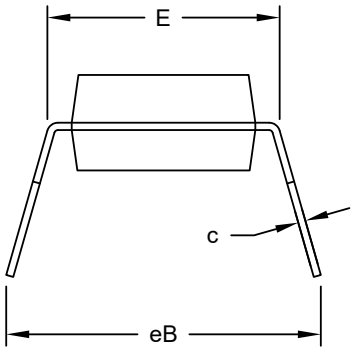



TOP VIEW






SIDE VIEW



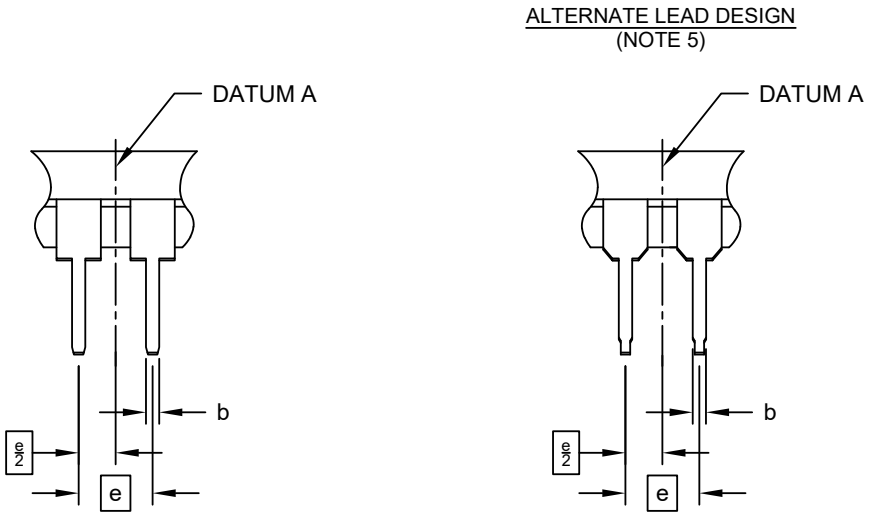

END VIEW

Microchip Technology Drawing No. C04-018-P Rev G Sheet 1 of 2


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## 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | - | - | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | - | - |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | - | - | .430 |

Notes:

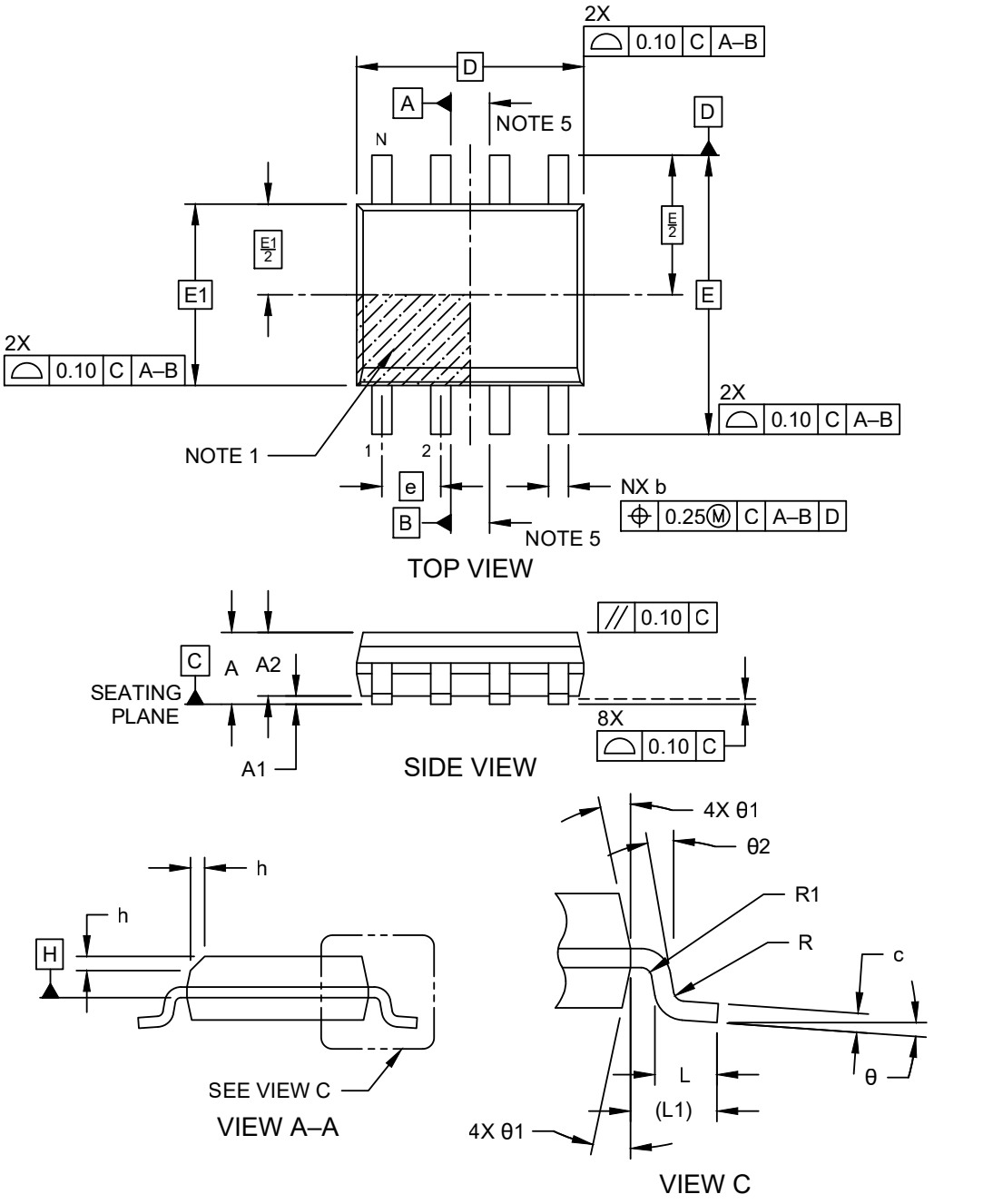
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev G Sheet 2 of 2


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## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

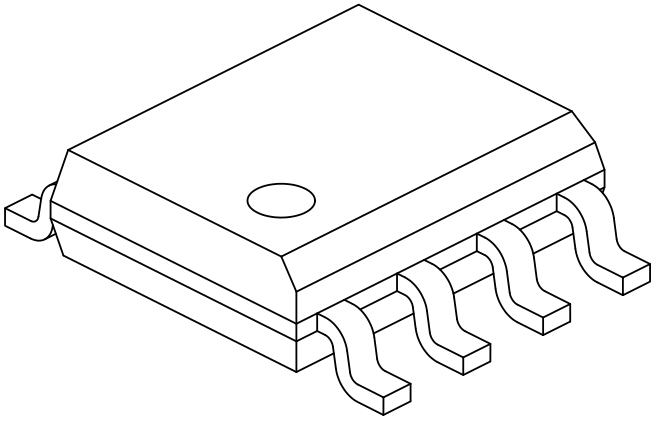



Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 1 of 2


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## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | - |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Lead Bend Radius | R | 0.07 | – | – |
| Lead Bend Radius | R1 | 0.07 | – | – |
| Foot Angle | θ | 0° | – | 8° |
| Mold Draft Angle | θ1 | 5° | – | 15° |
| Lead Angle | θ2 | 0° | – | – |

Notes:

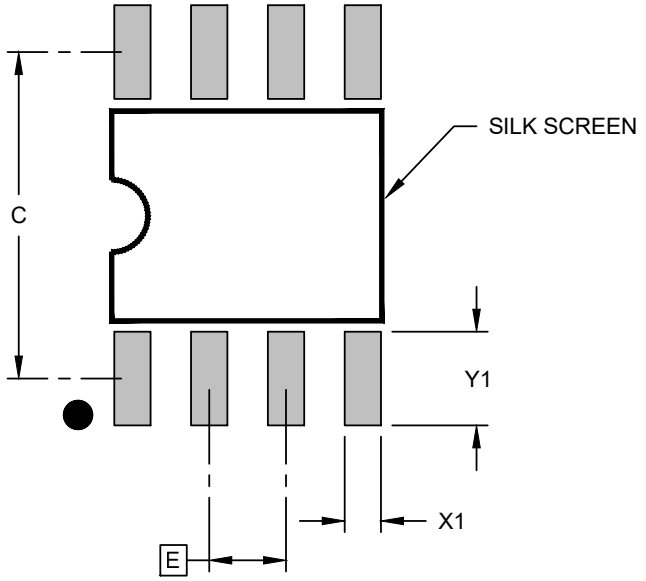
1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 2 of 2


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## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

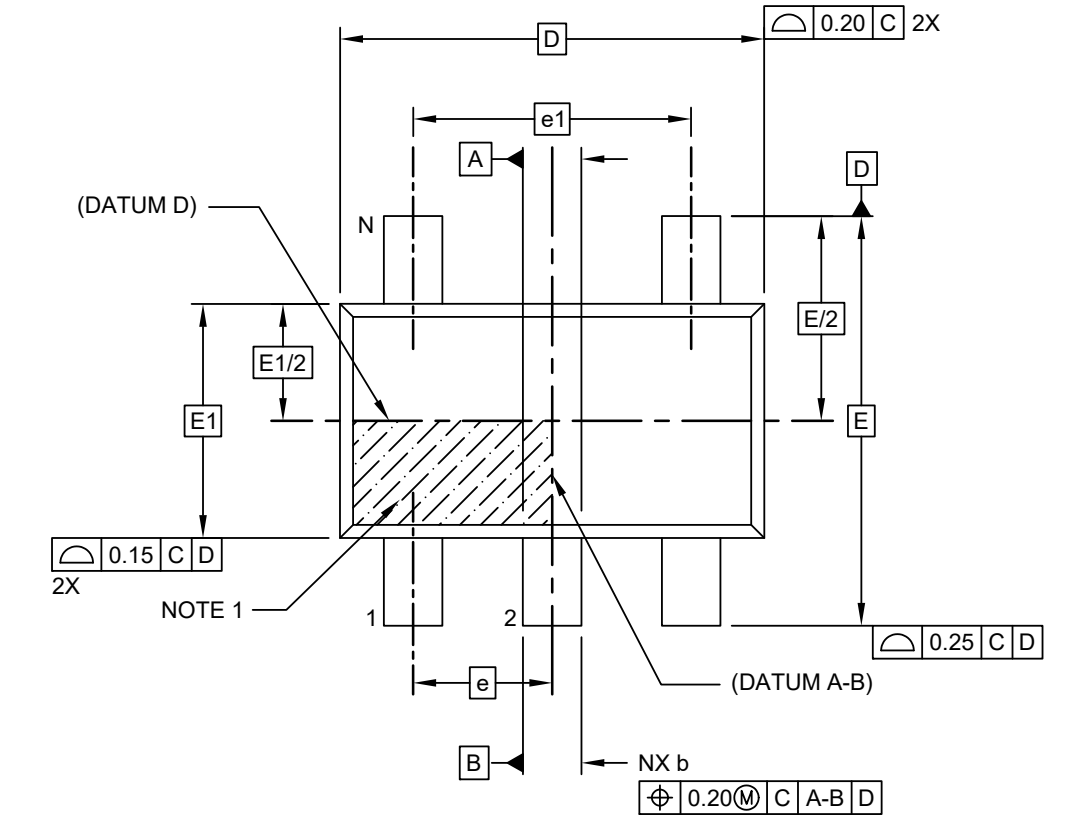
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-02057-SN Rev L

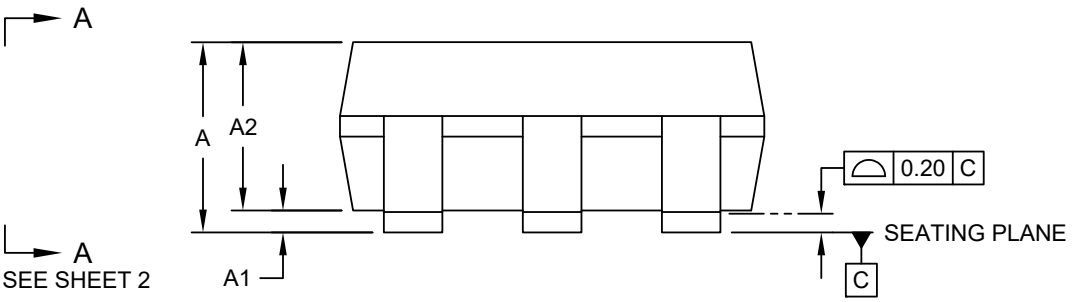

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## 5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW



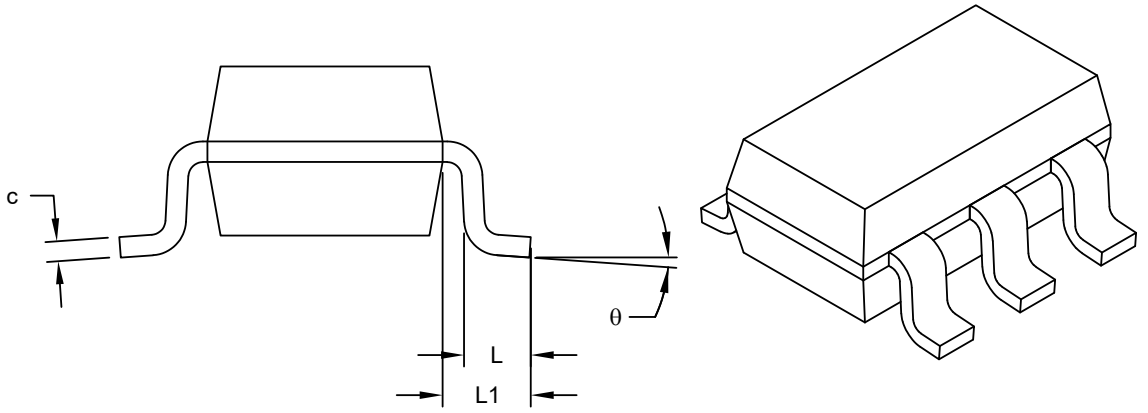

SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev H Sheet 1 of 2


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## 5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




VIEW A-A
SHEET 1

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 5 | |
| Pitch | e | | 0.95 BSC | |
| Outside lead pitch | e1 | | 1.90 BSC | |
| Overall Height | A | 0.90 | - | 1.45 |
| Molded Package Thickness | A2 | 0.89 | - | 1.30 |
| Standoff | A1 | - | - | 0.15 |
| Overall Width | E | | 2.80 BSC | |
| Molded Package Width | E1 | | 1.60 BSC | |
| Overall Length | D | | 2.90 BSC | |
| Foot Length | L | 0.30 | - | 0.60 |
| Footprint | L1 | | 0.60 REF | |
| Foot Angle | θ | 0° | - | 10° |
| Lead Thickness | c | 0.08 | - | 0.26 |
| Lead Width | b | 0.20 | - | 0.51 |

Notes:

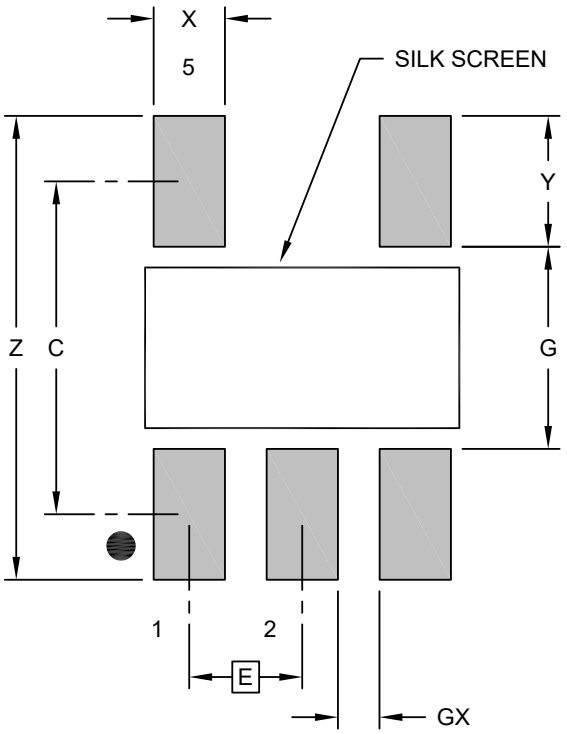
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev H Sheet 2 of 2


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## 5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

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RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.95 BSC | |
| Contact Pad Spacing | C | | 2.80 | |
| Contact Pad Width (X5) | X | | | 0.60 |
| Contact Pad Length (X5) | Y | | | 1.10 |
| Distance Between Pads | G | 1.70 | | |
| Distance Between Pads | GX | 0.35 | | |
| Overall Width | Z | | | 3.90 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

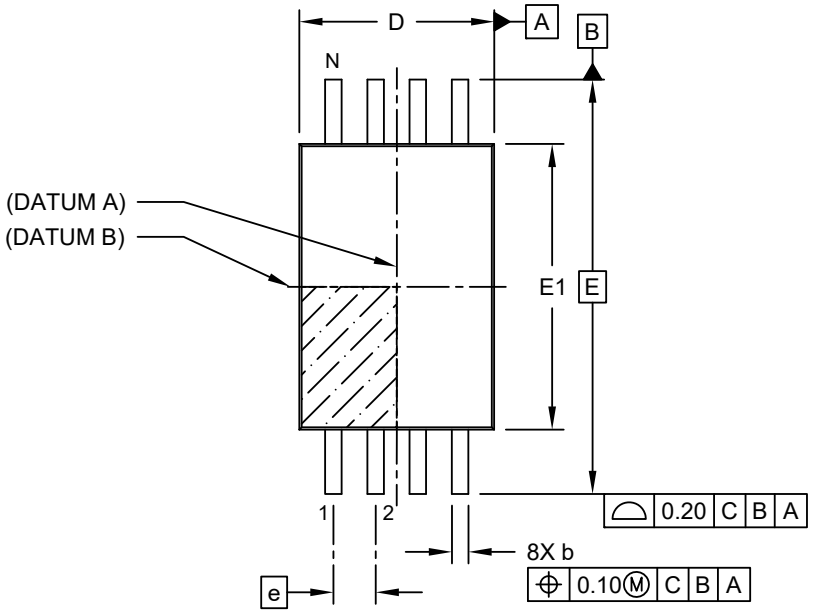
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-OT Rev H

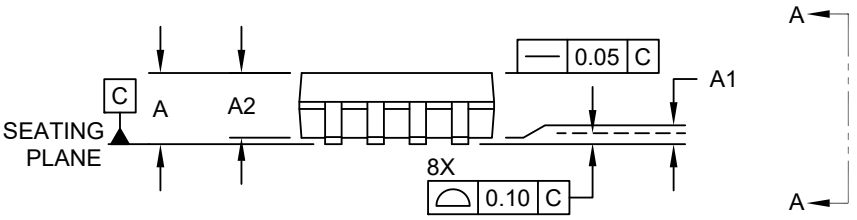

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## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

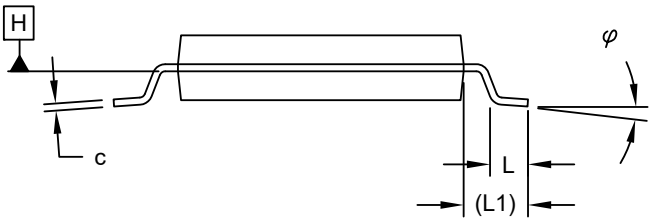
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




TOP VIEW




SIDE VIEW



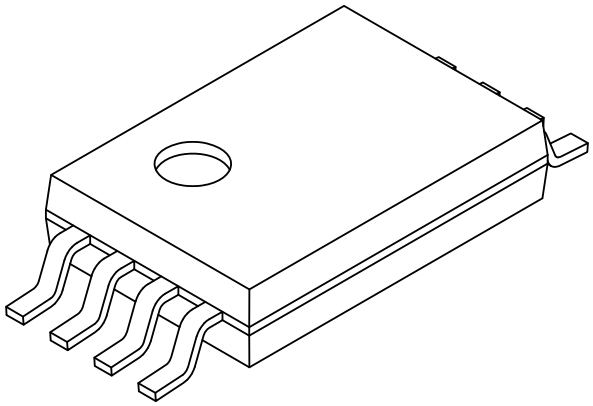

VIEW A-A

Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2


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## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | - | - | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | - | - |
| Overall Width | E | | 6.40 BSC | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Overall Length | D | 2.90 | 3.00 | 3.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Lead Thickness | c | 0.09 | - | 0.25 |
| Foot Angle | φ | 0° | 4° | 8° |
| Lead Width | b | 0.19 | - | 0.30 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

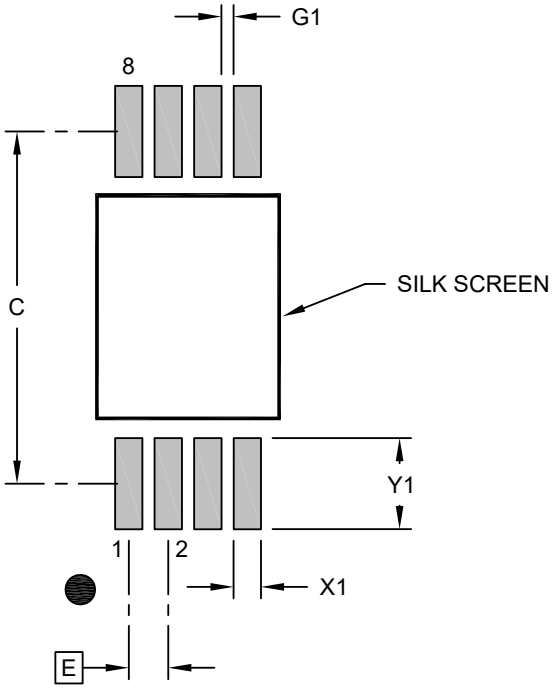
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2


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## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 5.80 | |
| Contact Pad Width (X8) | X1 | | | 0.45 |
| Contact Pad Length (X8) | Y1 | | | 1.50 |
| Contact Pad to Center Pad (X6) | G1 | 0.20 | | |

Notes:

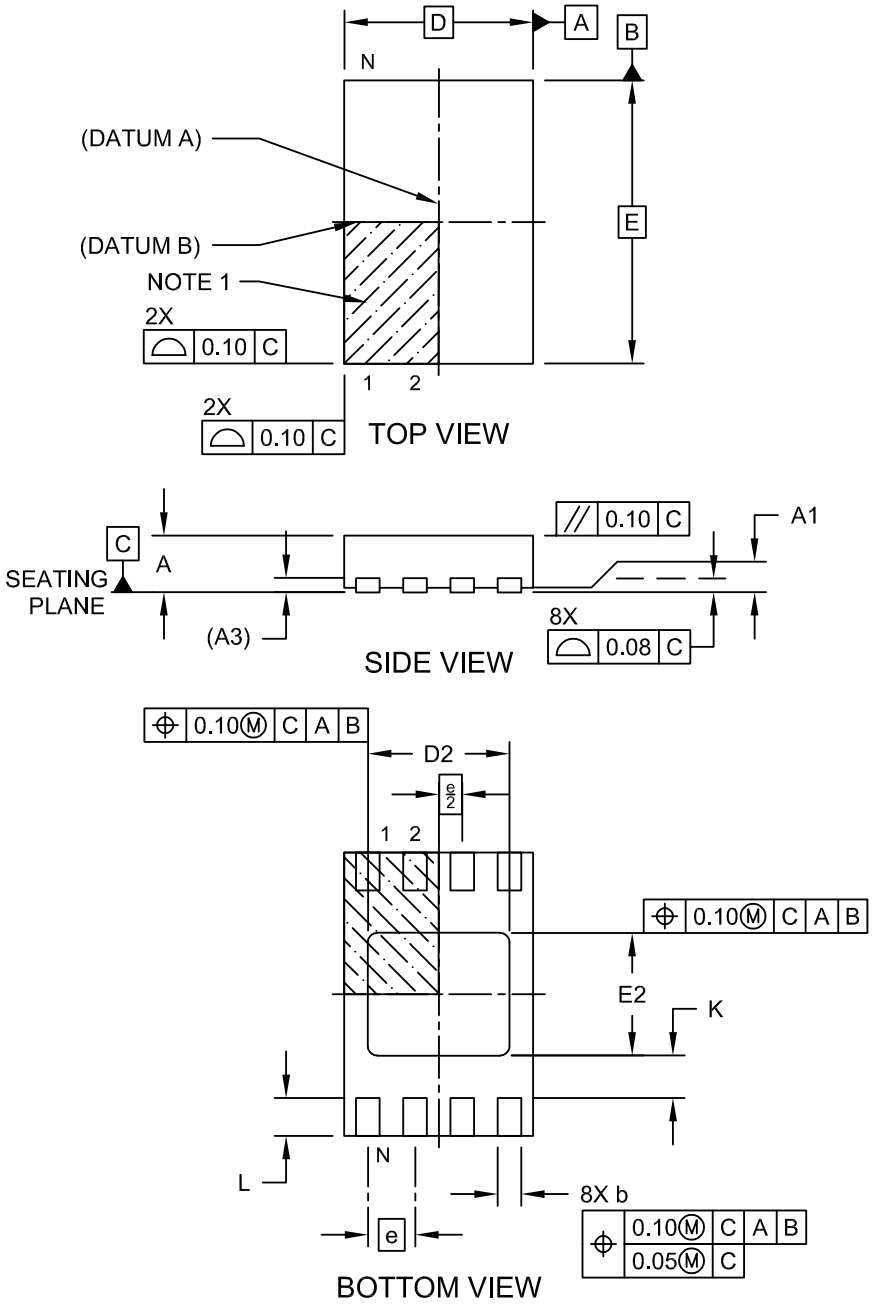
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B


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## 8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
## Atmel Legacy Global Package Code YNZ

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

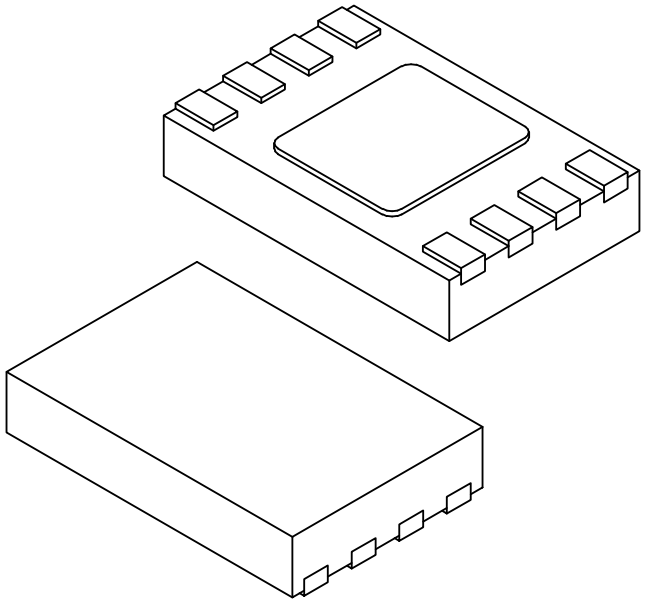



Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 1 of 2


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## 8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
## Atmel Legacy Global Package Code YNZ

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.50 | 0.55 | 0.60 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.152 REF | |
| Overall Length | D | | 2.00 BSC | |
| Exposed Pad Length | D2 | 1.40 | 1.50 | 1.60 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.20 | 1.30 | 1.40 |
| Terminal Width | b | 0.18 | 0.25 | 0.30 |
| Terminal Length | L | 0.25 | 0.35 | 0.45 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

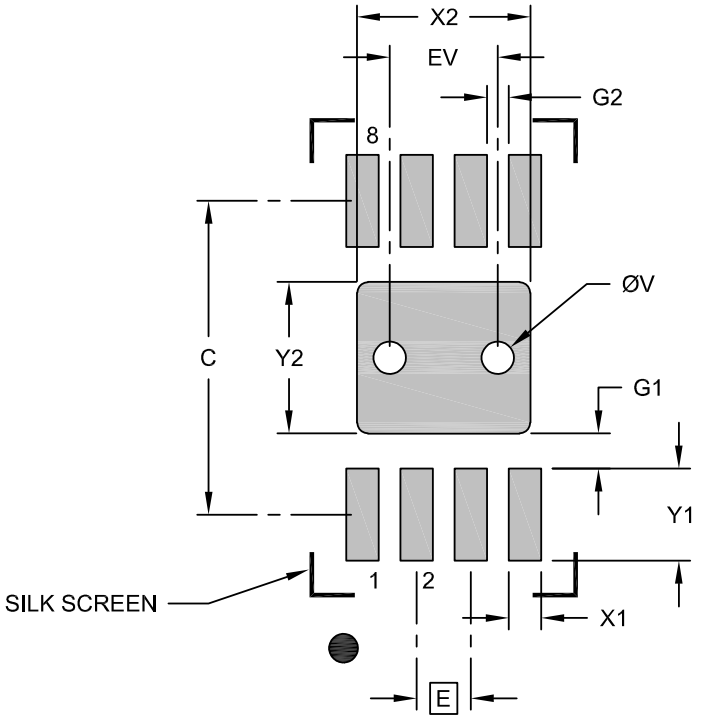
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 2 of 2


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## 8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy Global Package Code YNZ

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 1.60 |
| Optional Center Pad Length | Y2 | | | 1.40 |
| Contact Pad Spacing | C | | 2.90 | |
| Contact Pad Width (X8) | X1 | | | 0.30 |
| Contact Pad Length (X8) | Y1 | | | 0.85 |
| Contact Pad to Center Pad (X8) | G1 | 0.33 | | |
| Contact Pad to Contact Pad (X6) | G2 | 0.20 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23355-Q4B Rev C


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# 11. Revision History

### Revision B (October 2026)

Removed the VFBGA package due to its end-of-life status. Made minor editorial revisions throughout the document.

### Revision A (November 2018)

Updated to the Microchip template. Microchip DS20006111 replaces Atmel document 8700. Corrected $t_{LOW}$ typo from 400 ns to 500 ns. Corrected $t_{AA}$ typo from 550 ns to 450 ns. Updated Part Marking Information. Updated the "Software Reset" section. Added ESD rating. Removed lead finish designation. Updated trace code format in package markings. Added a figure for “System Configuration Using Two-Wire Serial EEPROMs”. Updated "Block Diagram" figure. Added POR recommendations section. Made clarification updates throughout. Updated the 8U3-1 VFBGA package drawing. Updated the PDIP, SOIC, TSSOP, SOT-23 and UDFN package drawings to Microchip format.

### Atmel Document 8700 Revision H (December 2016)

Moved backside mark (YMXX) to front side line 2. Added @ = Country of Assembly.

### Atmel Document 8700 Revision G (January 2015)

Added the UDFN extended quantity option. Updated part markings, package drawings, ordering information, template and document organization.

### Atmel Document 8700 Revision F (June 2012)

Corrected ordering codes. Removed WDT from ordering code detail. Updated Atmel logos and disclaimer page.

### Atmel Document 8700 Revision E (May 2012)

Updated data sheet template. Added AT24C01C to document. Reduced all ISB from legacy values. Increased 1 MHz frequency range to include 2.5V operation. Updated package drawings to latest versions (where applicable). Updated selected waveforms.

### Atmel Document 8700 Revision D (August 2010)

Changed AT24C02C-XHM part marking from C02CM@ to 02CM @.

### Atmel Document 8700 Revision C (July 2010)

Changed Atmel AT24C02C-TSUM-T to Atmel AT24C02C-STUM-T, AT24C02CY6-MAHM-T to Atmel AT24C02C-MAHM-T and AT24C02CU3-CUM-T to Atmel AT24C02C-CUM-T. Changed TS = SOT-23 to ST = SOT-23.

### Atmel Document 8700 Revision B (February 2010)

Corrected catalog numbering scheme and ordering information.

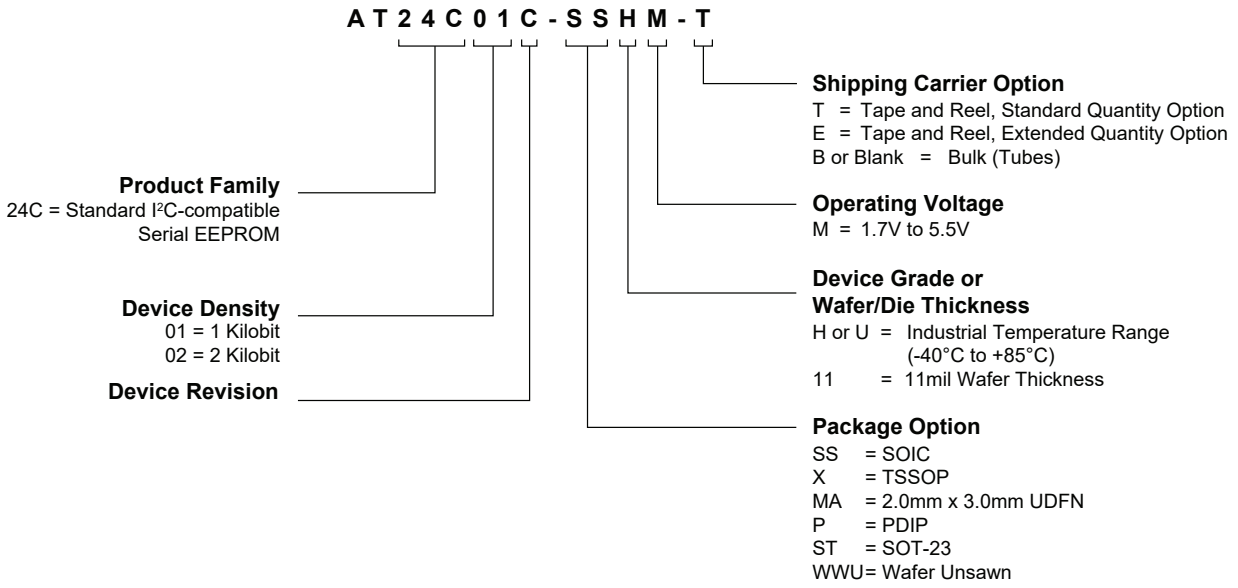
### Atmel Document 8700 Revision A (December 2009)

Initial release of this document.


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# 12. Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.




**Note:** Refer to automotive data sheet for automotive grade ordering information.

Examples

| Device | Package | Package Drawing Code | Package Option | Shipping Carrier Option | Device Grade |
|---|---|---|---|---|---|
| AT24C01C-PUM | PDIP | P | P | Bulk (Tubes) | Industrial Temperature (-40°C to 85°C) |
| AT24C01C-SSHM-B | SOIC | SN | SS | Bulk (Tubes) | |
| AT24C01C-SSHM-T | SOIC | SN | SS | Tape and Reel | |
| AT24C02C-SSHM-T | SOIC | SN | SS | Tape and Reel | |
| AT24C01C-XHM-B | TSSOP | ST | X | Bulk (Tubes) | |
| AT24C02C-XHM-T | TSSOP | ST | X | Tape and Reel | |
| AT24C01C-MAHM-T | UDFN | Q4B | MA | Tape and Reel | |
| AT24C01C-MAHM-E | UDFN | Q4B | MA | Extended Qty. Tape and Reel | |
| AT24C02C-MAHM-E | UDFN | Q4B | MA | Extended Qty. Tape and Reel | |
| AT24C02C-STUM-T | SOT-23 | OT | ST | Tape and Reel | |


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## Product Page Links

AT24C01C, AT24C02C


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