

# MOSFET – Single N-Channel, SUPERFET® V, FRFET® 600 V, 40 mΩ, 59 A

## NVHL040N60S5F

### Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM ( $R_{DS(on) max.} \times Q_{g typ.}$  &  $R_{DS(on) max.} \times E_{OSS}$ )
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	600	V
Gate-to-Source Voltage	DC	$\pm 30$	V
	AC ( $f > 1 \text{ Hz}$ )	$\pm 30$	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	59	A
	$T_C = 100^\circ\text{C}$	37	A
Power Dissipation	$T_C = 25^\circ\text{C}$	347	W
Pulsed Drain Current	$T_C = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	209
Pulsed Source Current (Body Diode)		$I_{SM}$	209
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	59	A
Single Pulse Avalanche Energy	( $I_L = 8.3 \text{ A}, R_G = 25 \Omega$ )	$E_{AS}$	574
Avalanche Current	$I_{AS}$	8.3	A
Repetitive Avalanche Energy (Note 1)	$E_{AR}$	3.47	mJ
MOSFET dv/dt	dvdt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)		70	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

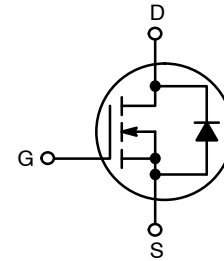
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $I_{SD} \leq 29.5 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq 400 \text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .

### THERMAL CHARACTERISTICS

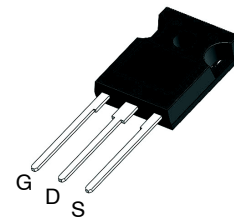
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max. (Notes 3, 4)	$R_{\theta JC}$	0.36	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient, Max. (Notes 3, 4)	$R_{\theta JA}$	40	

3. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
4. Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).

$V_{DSS}$	$R_{DS(on) MAX}$	$I_D MAX$
600 V	40 mΩ @ 10 V	59 A

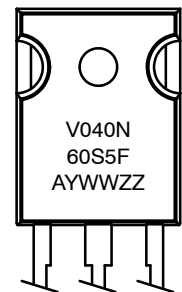


POWER MOSFET



TO-247-3LD  
CASE 340CX

### MARKING DIAGRAM



V040N60S5F = Specific Device Code  
A = Assembly Location  
YWW = Data Code (Year & Week)  
ZZ = Assembly Lot

### ORDERING INFORMATION

Device	Package	Shipping
NVHL040N60S5F	TO-247-3LD (Pb-Free)	30 Units / Tube

# NVHL040N60S5F

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 25°C	600			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	I <sub>D</sub> = 10 mA, Referenced to 25°C		581		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 650 V			10	μA
Gate-to-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V			±100	nA

### ON CHARACTERISTICS

Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 7.2 mA	3.2		4.8	V
Threshold Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T_J$	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 7.2 mA		-6.6		mV/°C
Static Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 29.5 A		32	40	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 29.5 A		59.5		S

### DYNAMIC CHARACTERISTICS

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 400 V, f = 1 MHz		6318		pF
Output Capacitance	C <sub>OSS</sub>			98.9		
Effective Output Capacitance	C <sub>OSS(eff.)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		1478		pF
Energy Related Output Capacitance	C <sub>OSS(er.)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		170		pF
Total Gate Charge at 10 V	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 400 V, I <sub>D</sub> = 29.5 A		115		nC
Gate-to-Source Gate Charge	Q <sub>GS</sub>			35.9		
Gate-to-Drain "Miller" Charge	Q <sub>GD</sub>			32.7		
Gate Resistance	R <sub>G</sub>	f = 1 MHz		4.5		Ω

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 400 V, I <sub>D</sub> = 29.5 A, R <sub>g</sub> = 2.2 Ω		49.6		ns
Turn-On Rise Time	t <sub>r</sub>			85.9		ns
Turn-Off Delay Time	t <sub>d(OFF)</sub>			110		ns
Turn-Off Fall Time	t <sub>f</sub>			2.5		ns

### SOURCE-DRAIN DIODE CHARACTERISTICS

Source-to-Drain Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 29.5 A		1.08	1.3	V
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>F</sub> /dt = 100 A/μs, I <sub>SD</sub> = 29.5 A		140		ns
Reverse Recovery Charge	Q <sub>RR</sub>			917		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NVHL040N60S5F

## TYPICAL CHARACTERISTICS

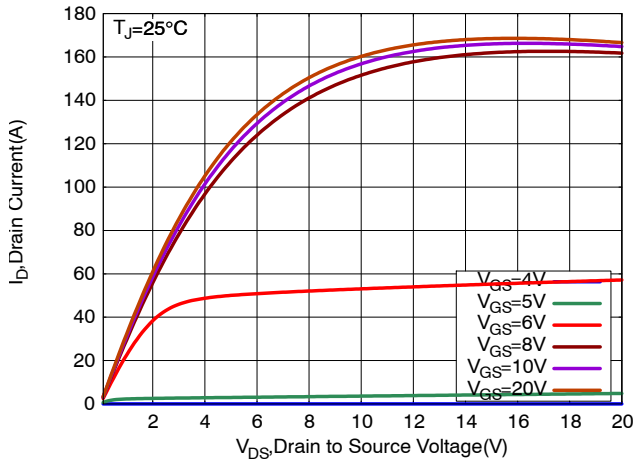


Figure 1. On-Region Characteristics

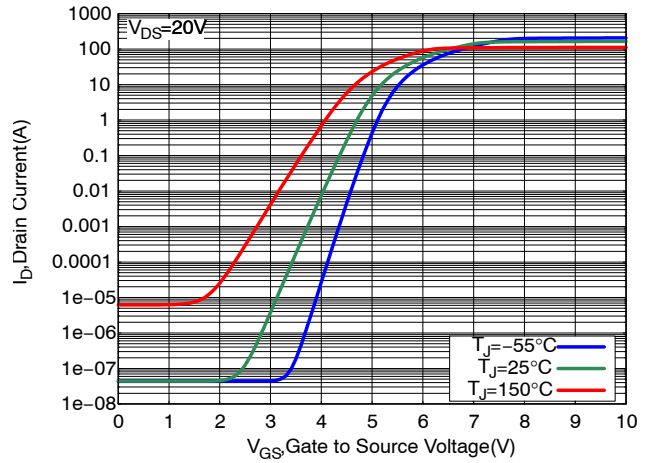


Figure 2. Transfer Characteristics

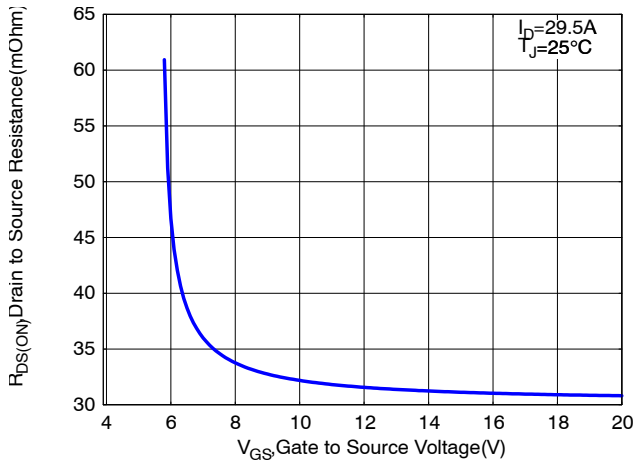


Figure 3. On-Resistance vs.  $V_{GS}$

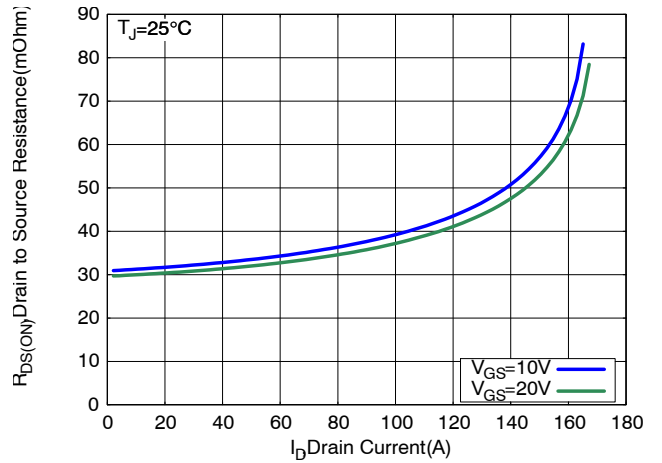


Figure 4. On-Resistance Variation vs. Drain Current and Gate Voltage

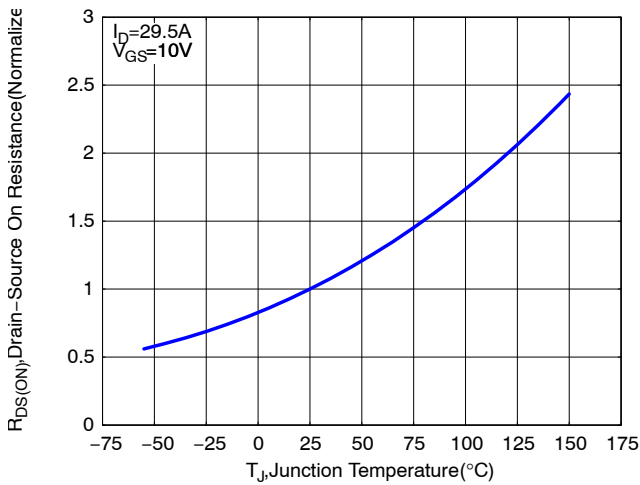


Figure 5. On-Resistance Variation with Temperature

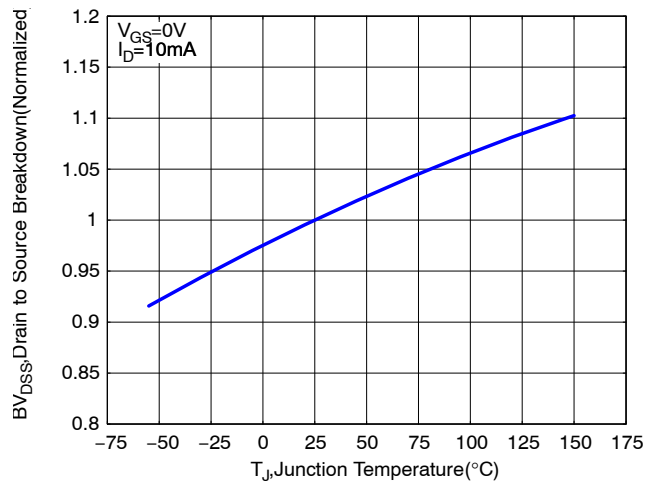


Figure 6. Breakdown Voltage Variation with Temperature

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## TYPICAL CHARACTERISTICS

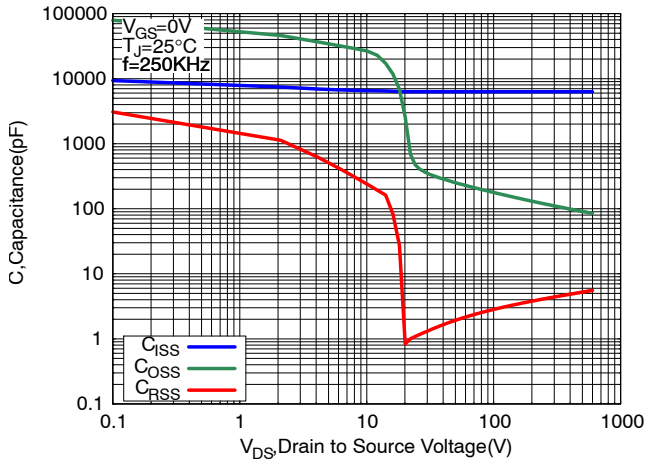


Figure 7. Capacitance Characteristics

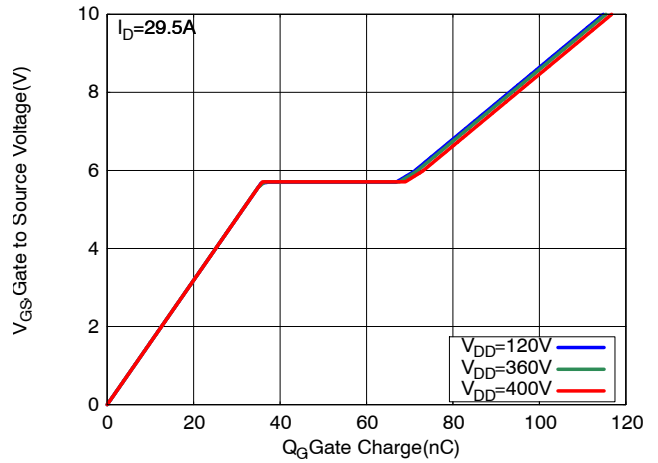


Figure 8. Gate-to-Source Voltage vs. Total Charge

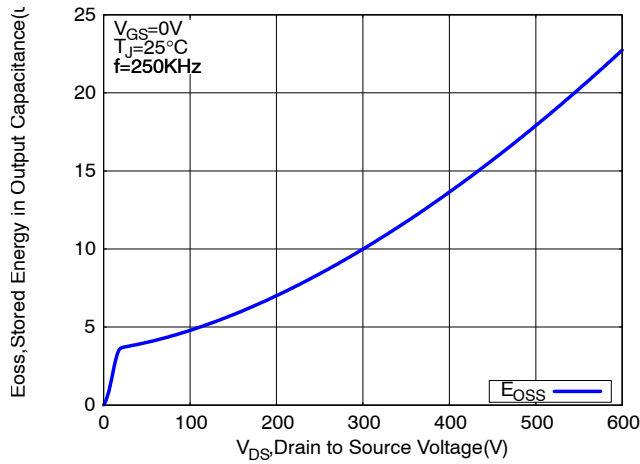


Figure 9. EOSS vs. Drain-to-Source Voltage

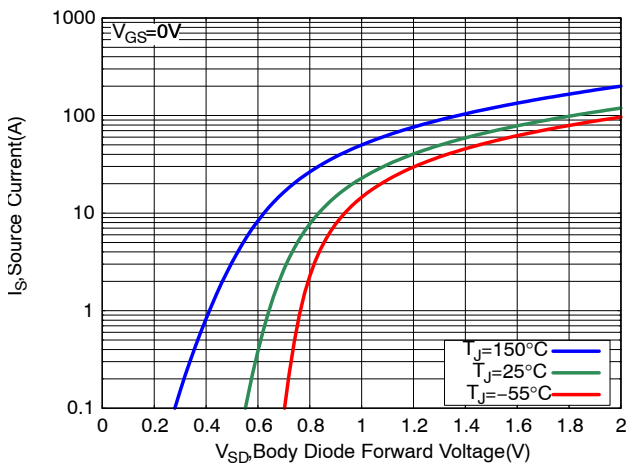


Figure 10. Diode Forward Voltage vs. Current

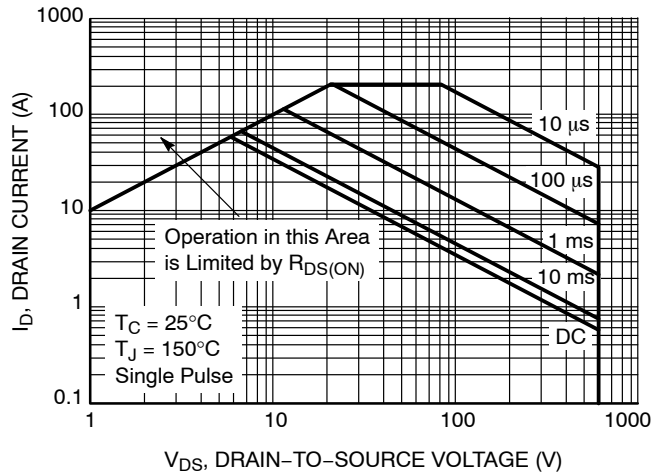


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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## TYPICAL CHARACTERISTICS

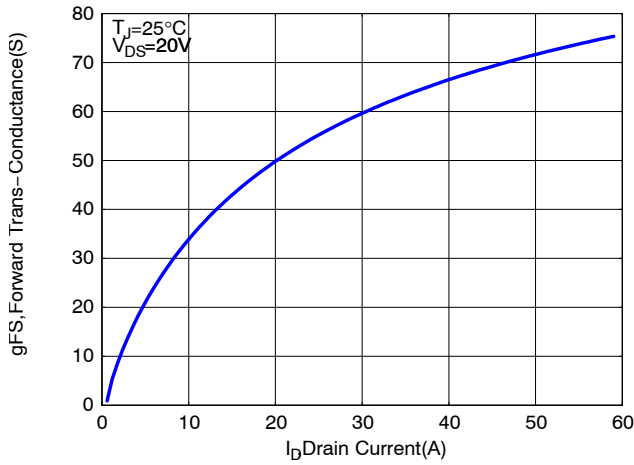


Figure 12.  $g_{FS}$  vs.  $I_D$

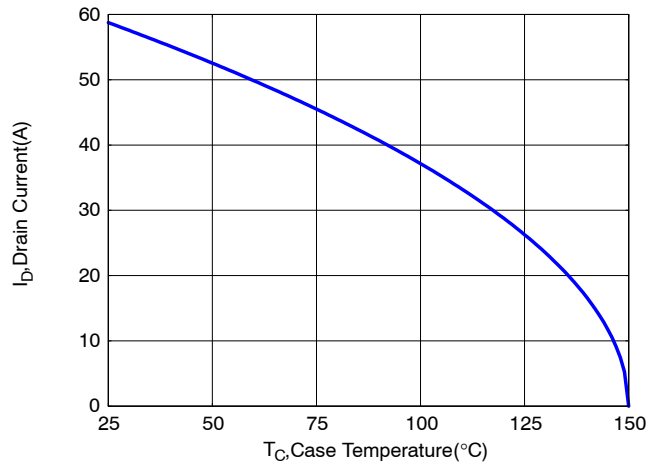


Figure 13. Maximum Current vs. Case Temperature

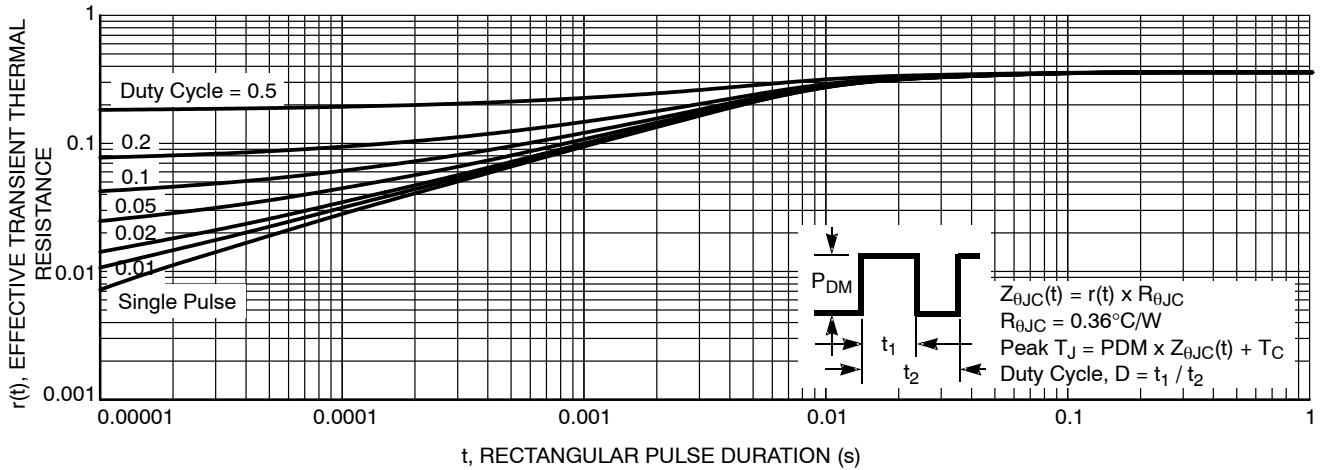


Figure 14. Thermal Response

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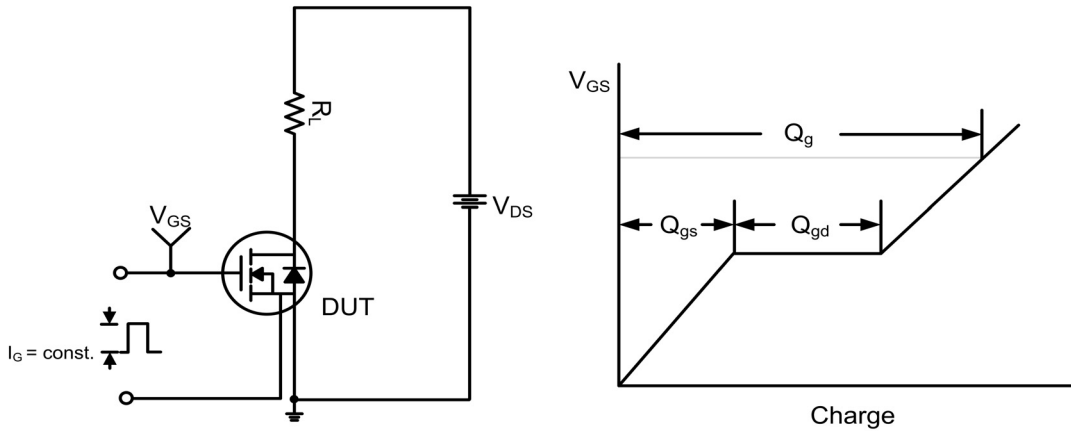


Figure 15. Gate Charge Test Circuit & Waveform

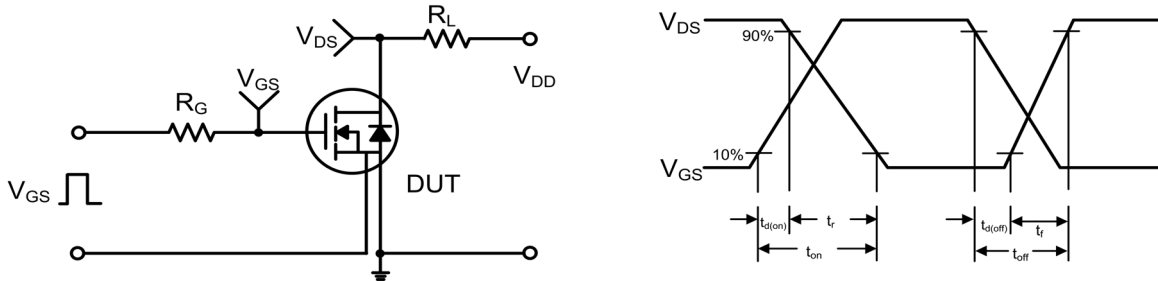


Figure 16. Resistive Switching Test Circuit & Waveforms

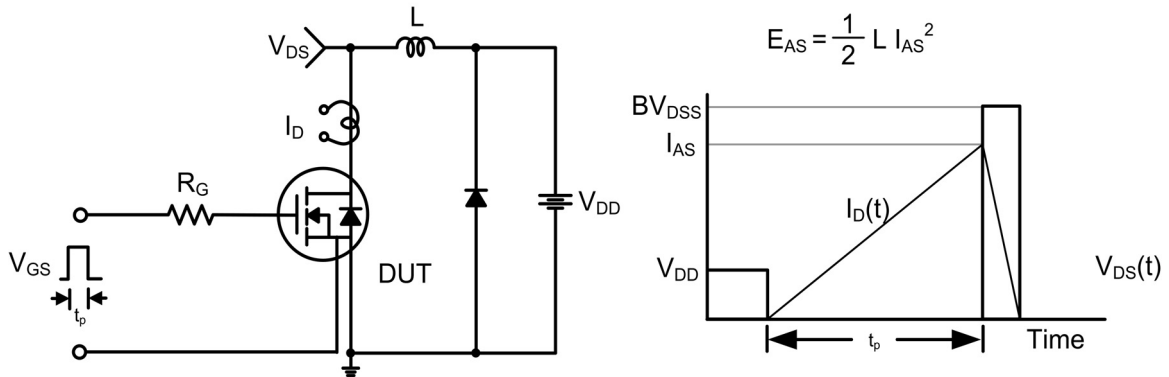
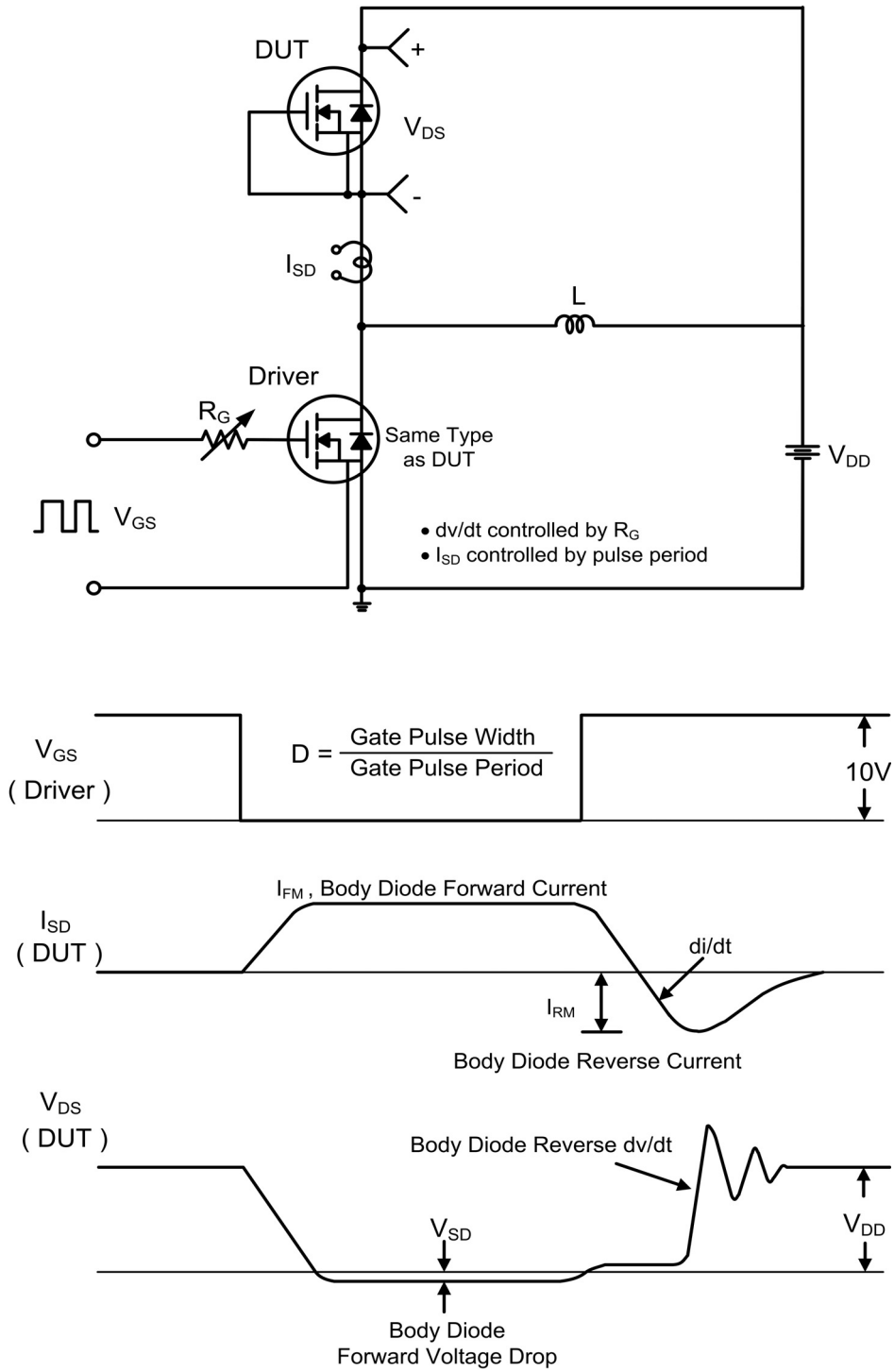


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

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**Figure 18. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

# MECHANICAL CASE OUTLINE

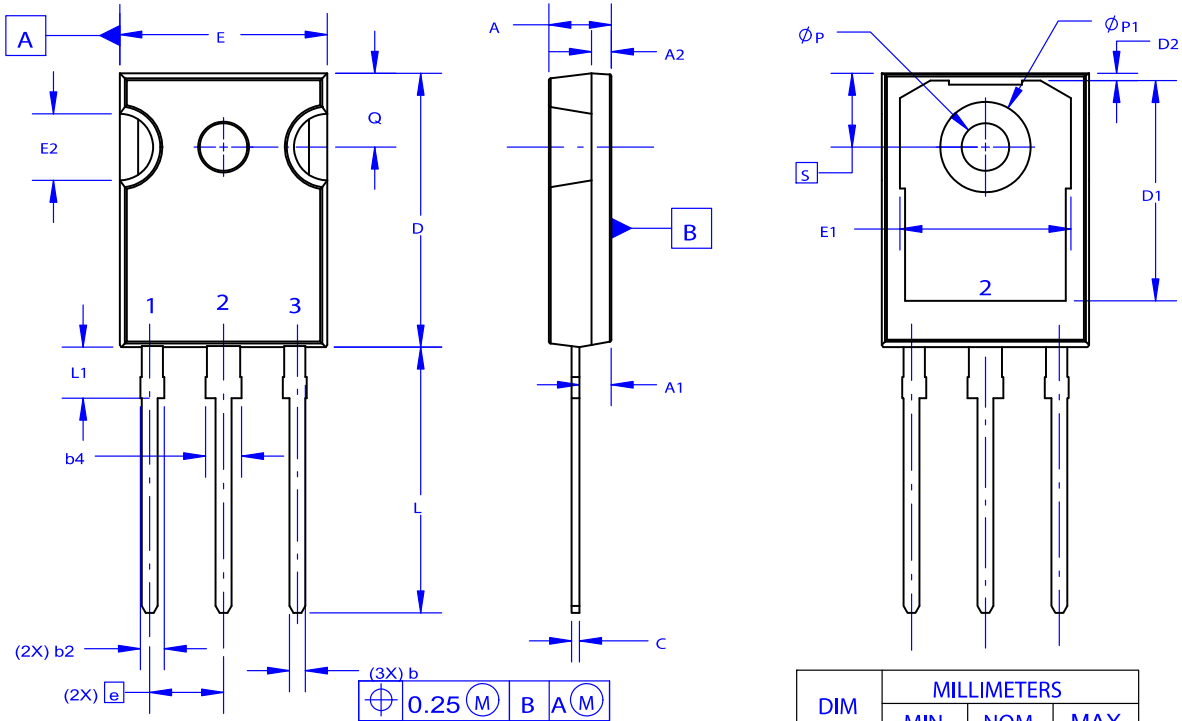
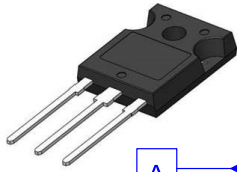
## PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD  
CASE 340CX  
ISSUE A

DATE 06 JUL 2020



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
∅P	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
∅P1	6.60	6.80	7.00

### GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>TO-247-3LD</b>	<b>PAGE 1 OF 1</b>

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