

MOSFET – Single N-Channel, SUPERFET® III, FRFET® 650 V, 75 A, 27.4 mΩ

NVH4L027N65S3F

Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM ($R_{DS(on)}$ max. $\times$ Q_g typ. & $R_{DS(on)}$ max. $\times$ E_{OSS})
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	650	V
Gate-to-Source Voltage – DC	V_{GSS}	± 30	V
Gate-to-Source Voltage – AC ($f > 1$ Hz)	V_{GSS}	± 30	V
Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	I_D	75	A
Drain Current – Continuous ($T_C = 100^\circ\text{C}$)	I_D	60	A
Drain Current – Pulsed (Note 3)	I_{DM}	187.5	A
Power Dissipation ($T_C = 25^\circ\text{C}$)	P_D	595	W
Power Dissipation – Derate Above 25°C	P_D	4.76	W/ $^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to $+150$	$^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 4)	E_{AS}	1610	mJ
Repetitive Avalanche Energy (Note 3)	E_{AR}	5.95	mJ
MOSFET dv/dt	dv/dt	100	V/ns
Peak Diode Recovery dv/dt (Note 5)	dv/dt	50	V/ns
Max. Lead Temperature for Soldering Purposes (1/8" from case for 5 s)	T_L	300	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max. (Notes 1, 2)	$R_{\theta JC}$	0.21	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient, Max. (Notes 1, 2)	$R_{\theta JA}$	40	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

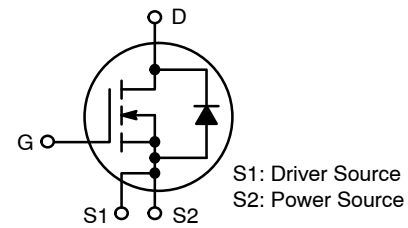
1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).
3. Repetitive rating: pulse-width limited by maximum junction temperature.
4. $I_{AS} = 15$ A, $R_G = 25$ Ω , starting $T_J = 25^\circ\text{C}$.
5. $I_{SD} \leq 37.5$ A, $di/dt \leq 200$ A/ μs , $V_{DD} \leq 400$ V, starting $T_J = 25^\circ\text{C}$.



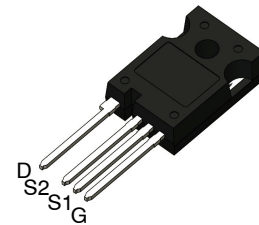
ON Semiconductor®

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V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
650 V	27.4 mΩ @ 10 V	75 A

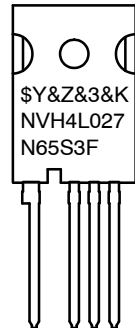


POWER MOSFET



TO-247-4LD
CASE 340CJ

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
 &Z = Assembly Plant Code
 &3 = Data Code (Year & Week)
 &K = Lot
 NVH4L027N65S3F = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NVH4L027N65S3F	TO-247-4LD (Pb-Free)	30 Units / Tube

NVH4L027N65S3F

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650			V
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 10 mA, T _J = 150°C	700			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	I _D = 20 mA, Referenced to 25°C		610		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 650 V			10	μA
		V _{DS} = 520 V, T _C = 125°C		590		
Gate-to-Body Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 3 mA	3.0		5.0	V
Threshold Temperature Coefficient	$\Delta V_{GS(th)} / \Delta T_J$	V _{GS} = V _{DS} , I _D = 3 mA		-7.3		mV/°C
Static Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 35 A		21.5	27.4	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 20 V, I _D = 37.5 A		57		S

DYNAMIC CHARACTERISTICS

Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 400 V, f = 1 MHz		7780		pF
Output Capacitance	C _{oss}			200		
Reverse Transfer Capacitance	C _{rss}			26		
Effective Output Capacitance	C _{oss(eff.)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		1880		pF
Energy Related Output Capacitance	C _{oss(er.)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		347		pF
Total Gate Charge at 10 V	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 400 V, I _D = 37.5 A (Note 6)		227		nC
Threshold Gate Charge	Q _{G(TH)}			35		
Gate-to-Source Gate Charge	Q _{GS}			67		
Gate-to-Drain "Miller" Charge	Q _{GD}			87		
Equivalent Series Resistance	ESR	f = 1 MHz		2.2		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 400 V, I _D = 37.5 A, R _g = 2 Ω (Note 6)		42		ns
Turn-On Rise Time	t _r			34		ns
Turn-Off Delay Time	t _{d(off)}			153		ns
Turn-Off Fall Time	t _f			18		ns

SOURCE-DrAIN DIODE CHARACTERISTICS

Maximum Continuous Source-to-Drain Diode Forward Current	I _S	V _{GS} = 0 V			75	A
Maximum Pulsed Source-to-Drain Diode Forward Current	I _{SM}	V _{GS} = 0 V			187.5	A
Source-to-Drain Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _{SD} = 37.5 A			1.3	V
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, dI _F /dt = 100 A/μs, I _{SD} = 37.5 A		171		ns
Charge Time	t _a			141		
Discharge Time	t _b			29		
Reverse Recovery Charge	Q _{rr}			973		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

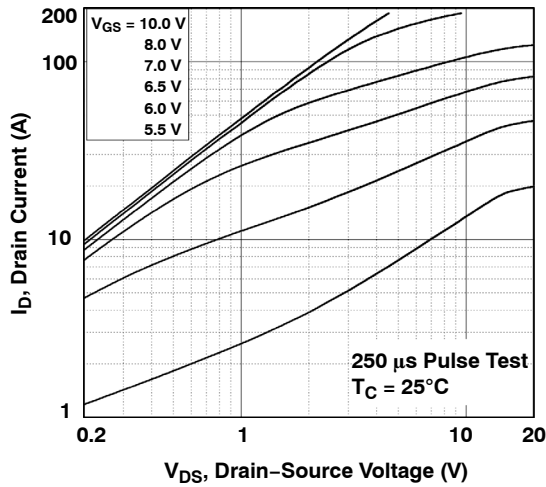


Figure 1. On-Region Characteristics

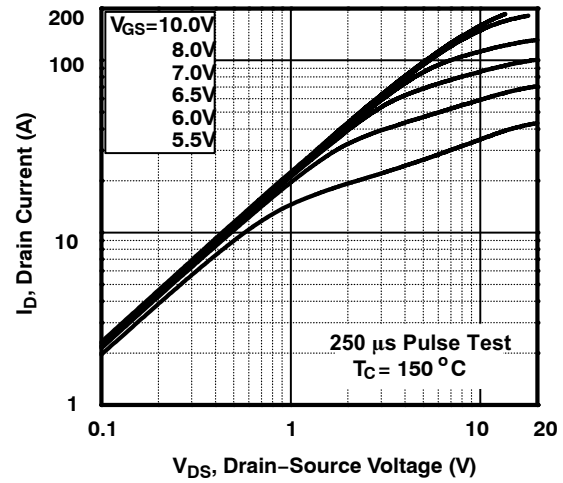


Figure 2. On-Region Characteristics

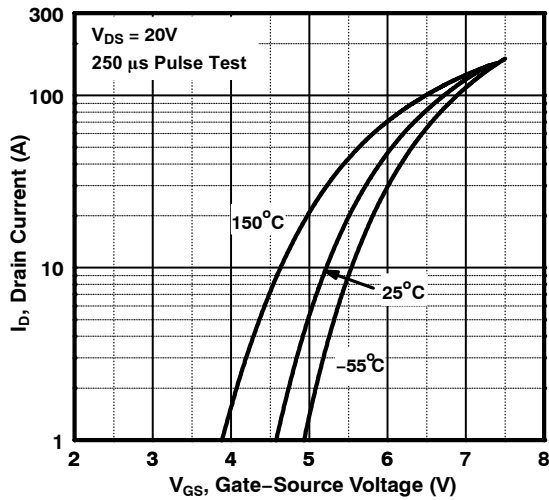


Figure 3. Transfer Characteristics

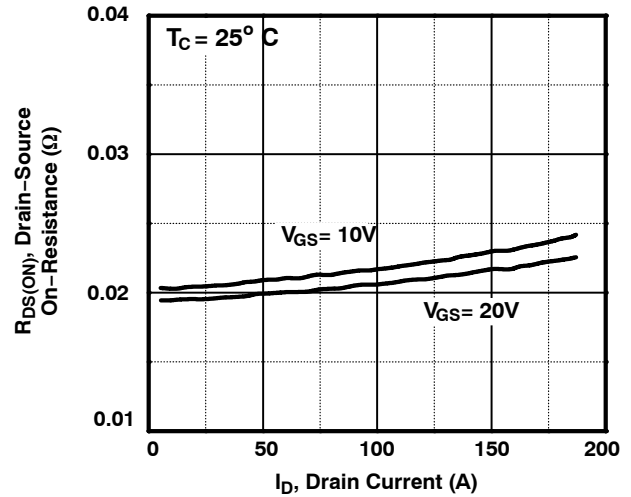


Figure 4. On-Resistance Variation vs. Drain Current and Gate Voltage

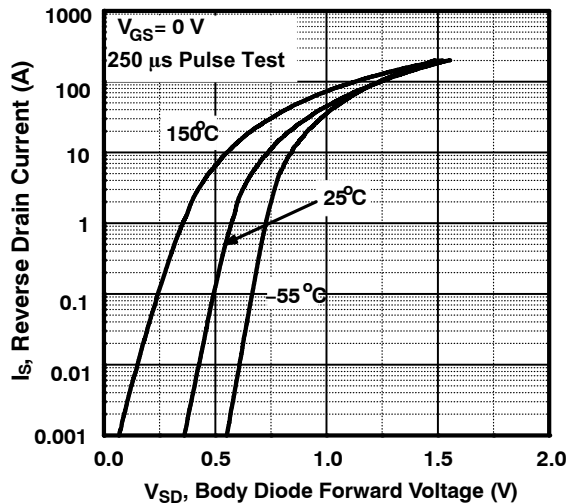


Figure 5. Body Diode Forward Voltage Variation vs. Source Current and Temperature

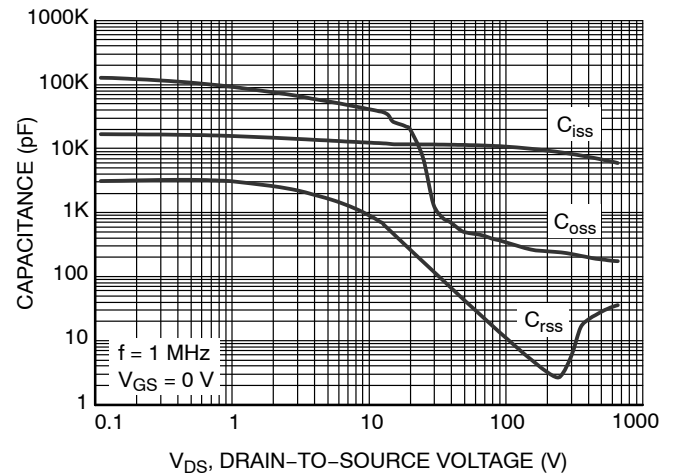


Figure 6. Capacitance Characteristics

TYPICAL CHARACTERISTICS

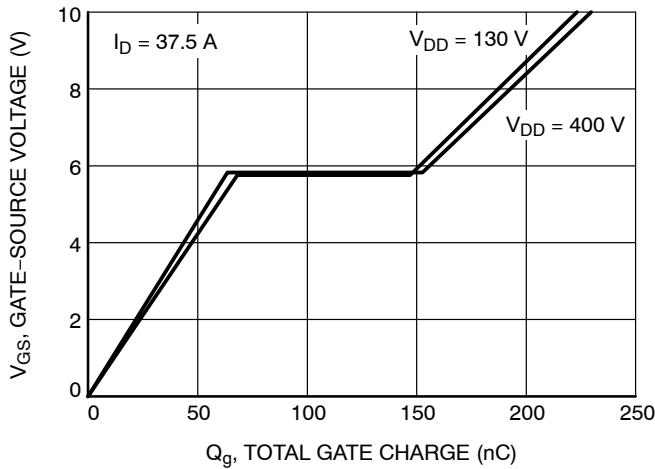


Figure 7. Gate Charge Characteristics

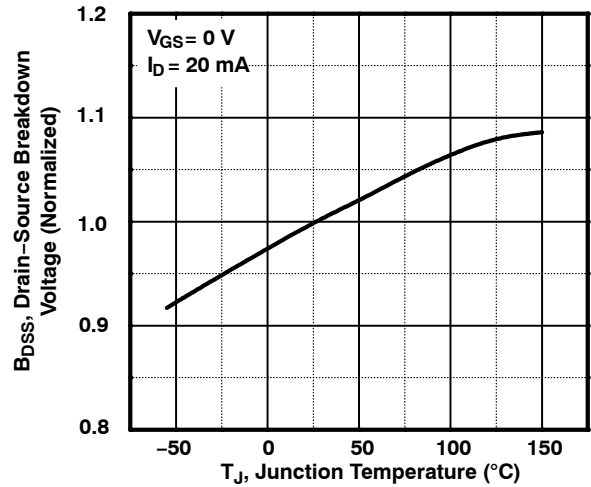


Figure 8. Breakdown Voltage Variation vs. Temperature

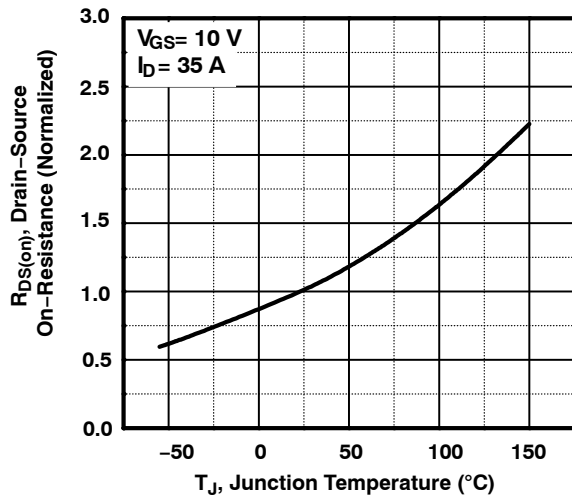


Figure 9. On-Resistance Variation vs. Temperature

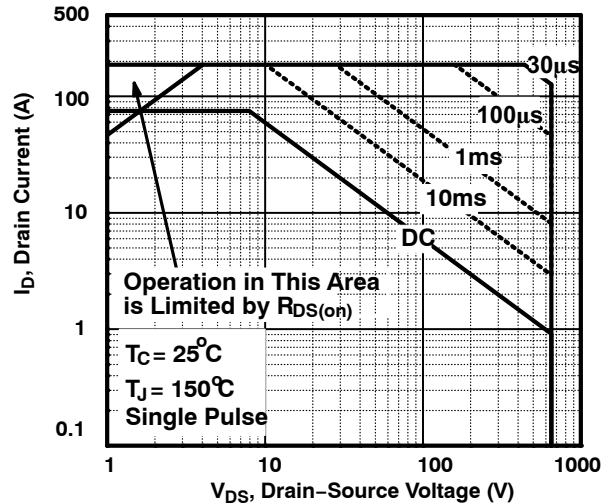


Figure 10. Maximum Safe Operating Area

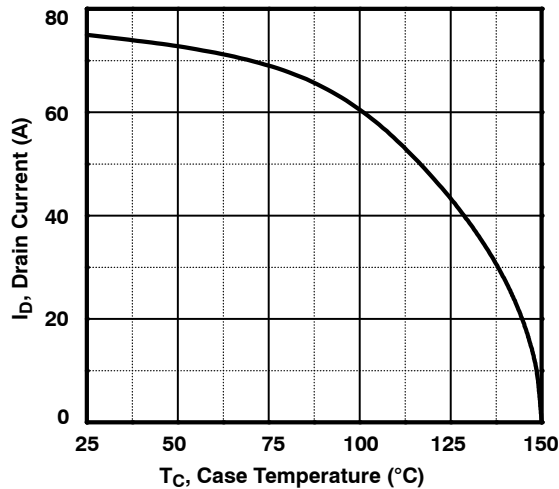


Figure 11. Maximum Drain Current vs. Case Temperature

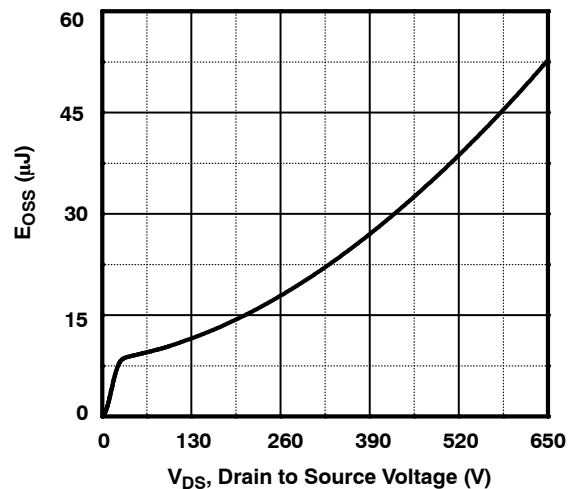


Figure 12. EOSS vs. Drain-to-Source Voltage

TYPICAL CHARACTERISTICS

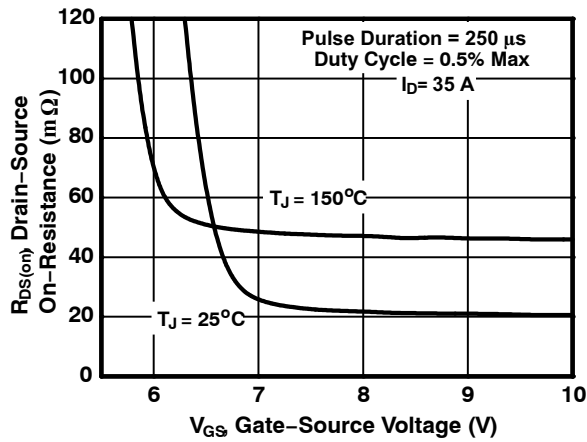


Figure 13. RDSON vs. Gate Voltage

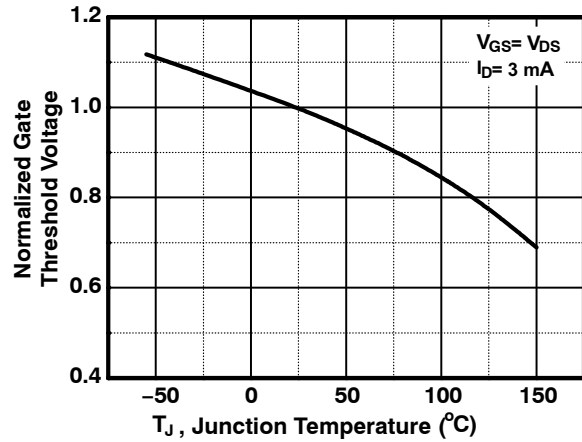
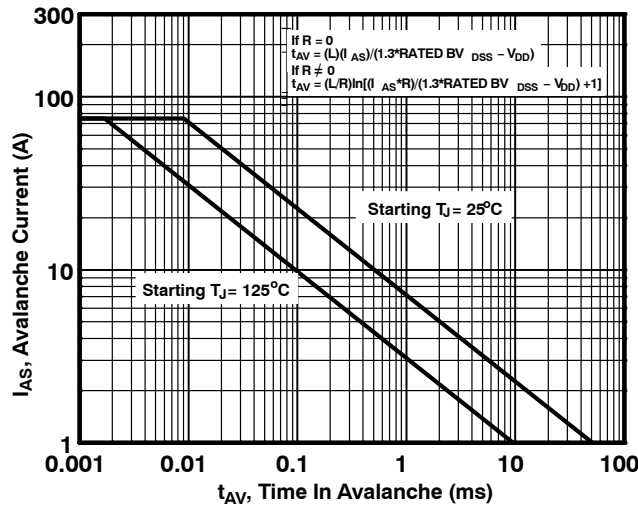


Figure 14. Normalized Gate Threshold Voltage vs. Temperature



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 15. Unclamped Inductive Switching Capability

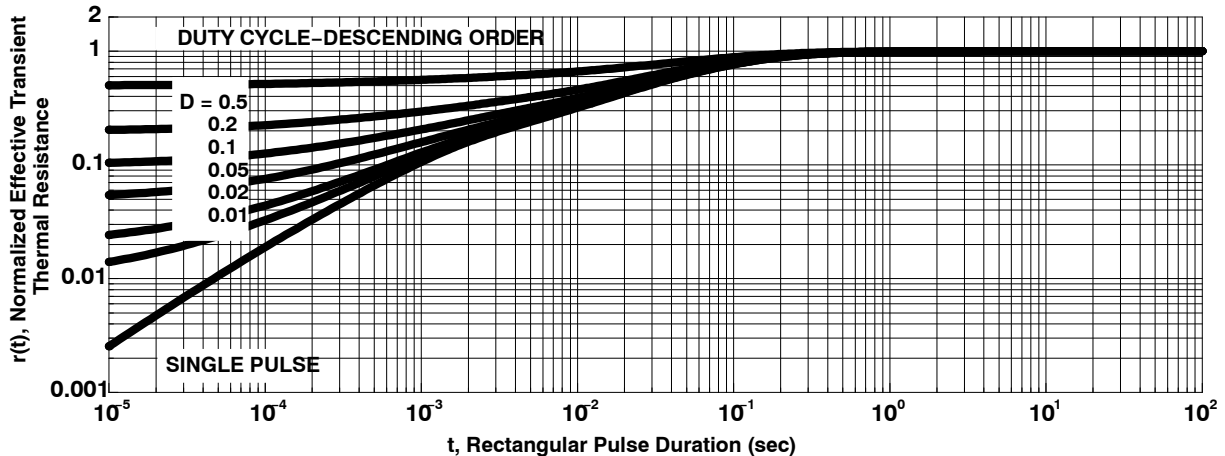
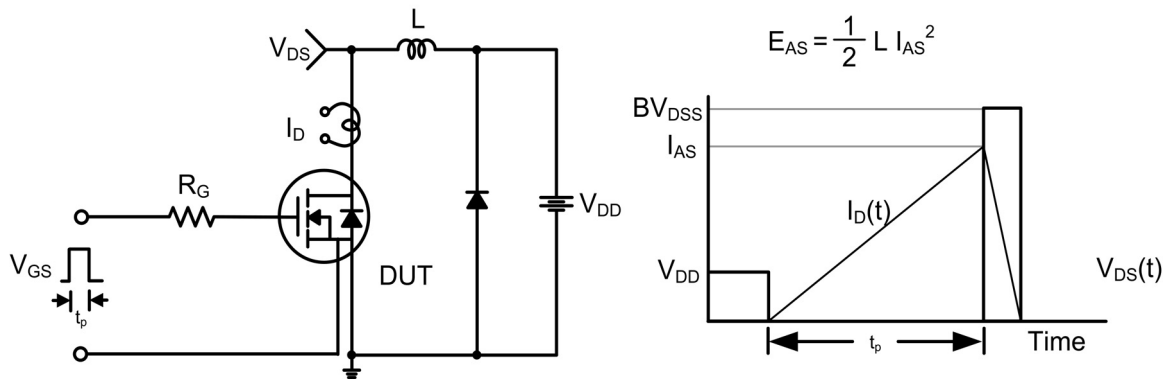
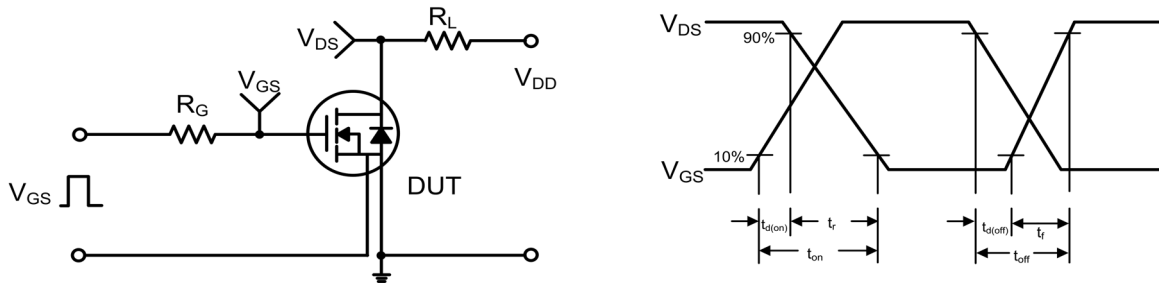
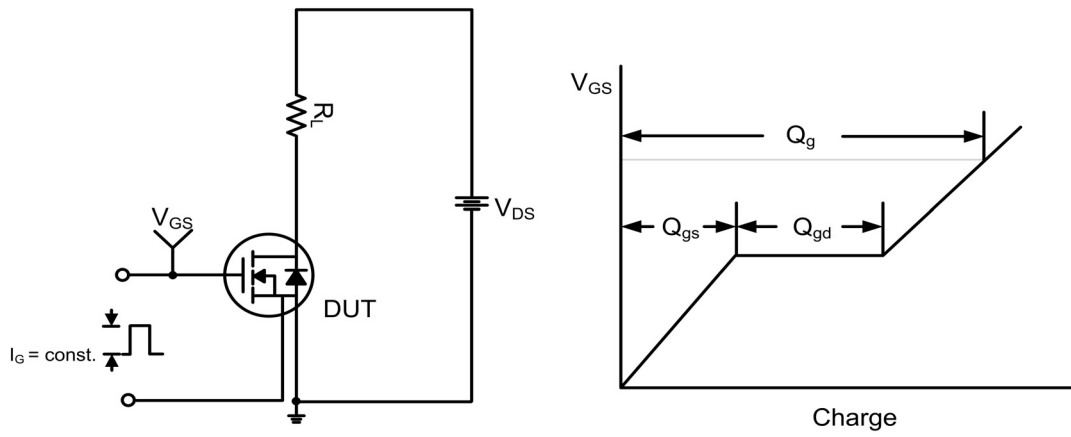


Figure 16. Transient Thermal Response Curve



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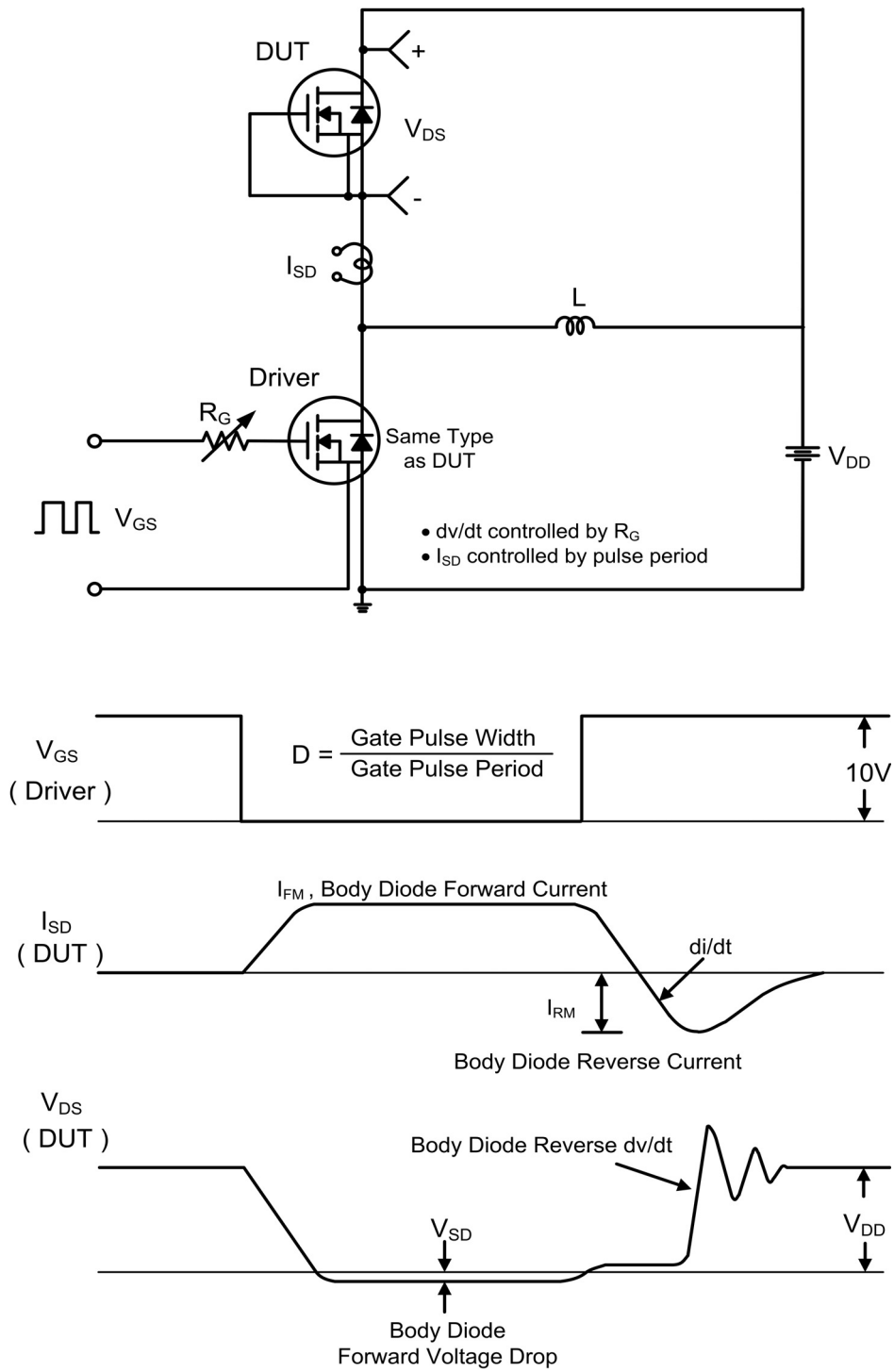
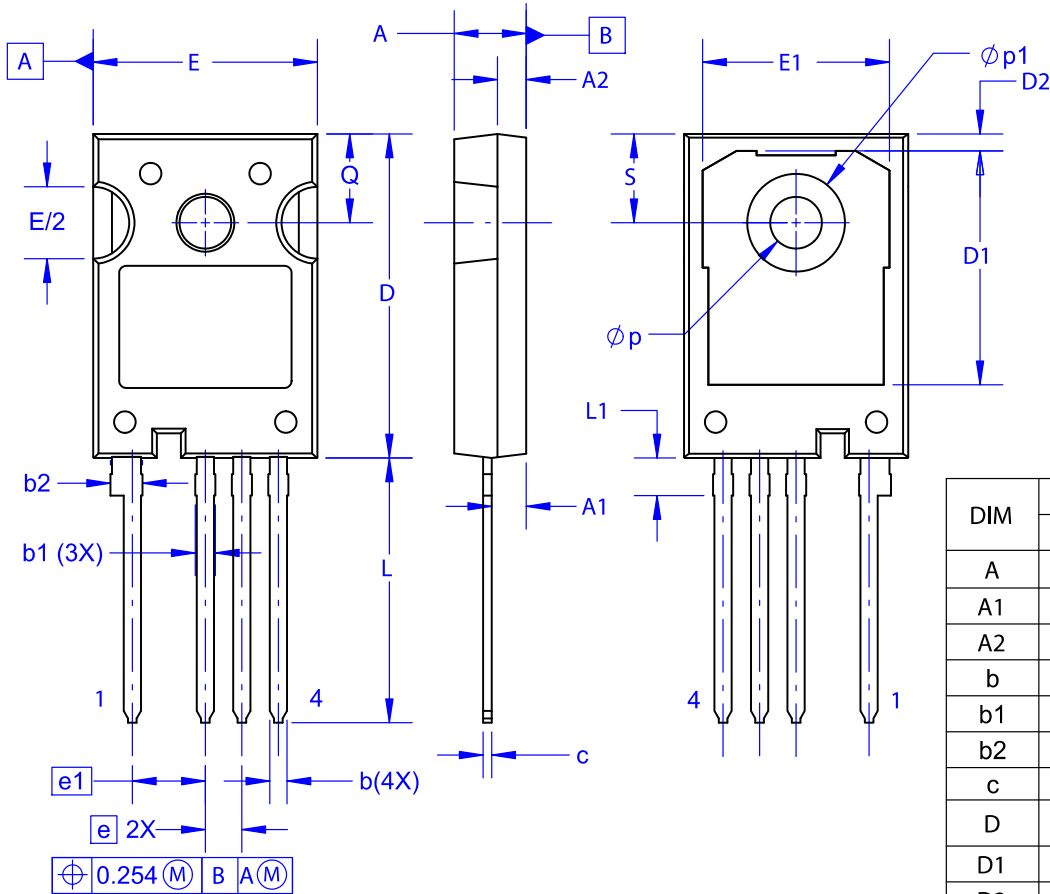


Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms

NVH4L027N65S3F

PACKAGE DIMENSIONS

TO-247-4LD
CASE 340CJ
ISSUE A



NOTES:

- A. NO INDUSTRY STANDARD APPLIES TO THIS PACKAGE.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5-2009.

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