MOSFET - Power, Single N-Channel, PQFN8
80 V, 32 A

NTMFS006N08MC

ON Semiconductor®

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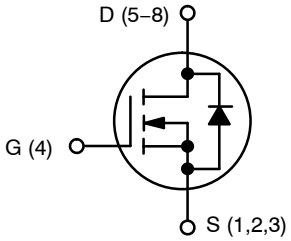
Features
- Advanced Package (5x6mm) with Excellent Thermal Conduction
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications
- Hot Swap Application
- Power Load Switch
- Battery Management and Protection

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	6.0 mΩ @ 10 V	32 A
80 V	17 mΩ @ 6 V	16 A



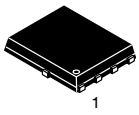
N−CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

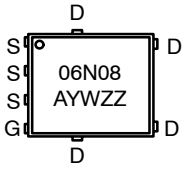
Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	80	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	T_C = 25°C	I_D	82	A
		T_C =85°C		59	
Power Dissipation $R_{\theta JC}$ (Note 3)		T_C = 25°C	P_D	78	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	T_A = 25°C	I_D	14.7	A
		T_A = 85°C		10.6	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		T_A = 25°C	P_D	2.5	W
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)		T_A = 25°C	I_D	9.3	A
		T_A = 85°C		6.7	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)		T_A = 25°C	P_D	1.0	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	216	A
Single Pulse Drain−to−Source Avalanche Energy (I_L = 32 A_{pk})			E_{AS}	51	mJ
Operating Junction and Storage Temperature Range			T_J, T_{STG}	−55 to +150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Surface−mounted on FR4 board using 1 in^2 pad, 2 oz Cu pad.
2. Surface−mounted on FR4 board using minimum pad size, 2 oz Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

MARKING DIAGRAMS



PQFN8
T1 SUFFIX
CASE 483AE



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceabililty

ORDERING INFORMATION
See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State	$R_{\theta JC}$	1.61	°C/W
Junction−to−Ambient − Steady State (Note 4)	$R_{\theta JA}$	50	
Junction−to−Ambient − Steady State (Note 5)	$R_{\theta JA}$	125	

4. Surface−mounted on FR4 board using 1 in^2 pad, 2 oz Cu pad.
5. Surface−mounted on FR4 board using minimum pad size, 2 oz Cu pad.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		80			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA. ref to 25°C			96.6		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 64 V	T_J = 25°C			1.0	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 6)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		2.0		4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 200 μA. ref to 25°C			−5		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 32 A		4.9	6.0	mΩ
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 6 V	I_D = 16 A		10.2	17	mΩ
Gate Resistance	R_G	T_A = 25°C			0.3		Ω
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz			2300		pF
Output Capacitance	C_{OSS}				710		
Reverse Transfer Capacitance	C_{RSS}				31		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 40 V; I_D = 32 A			30		nC
Threshold Gate Charge	$Q_{G(TH)}$				3.3		
Gate−to−Source Charge	Q_{GS}				10		
Gate−to−Drain Charge	Q_{GD}				6.0		
SWITCHING CHARACTERISTICS (Note 7)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 32 A, R_G = 2.5 Ω			13		ns
Rise Time	t_r				4		
Turn−Off Delay Time	$t_{d(OFF)}$				18		
Fall Time	t_f				4		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 32 A	T_J = 25°C		0.84	1.2	V
			T_J = 125°C		0.78		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 32 A			49.58		ns
Reverse Recovery Charge	Q_{RR}				51.4		nC

6. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
7. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

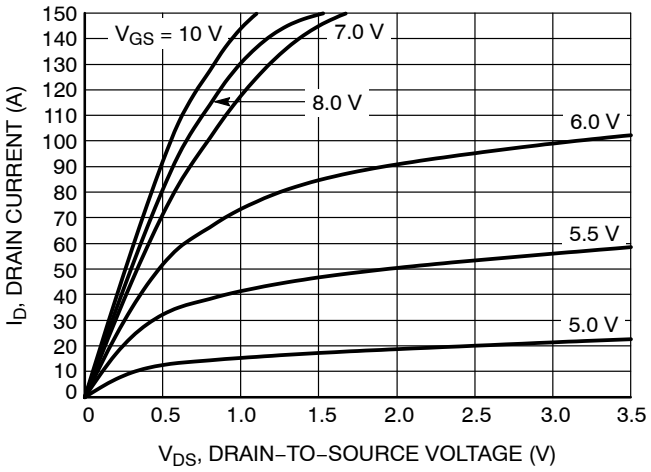


Figure 1. On−Region Characteristics

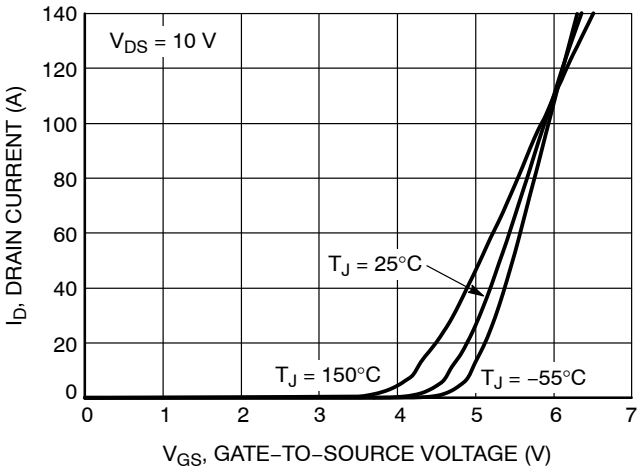


Figure 2. Transfer Characteristics

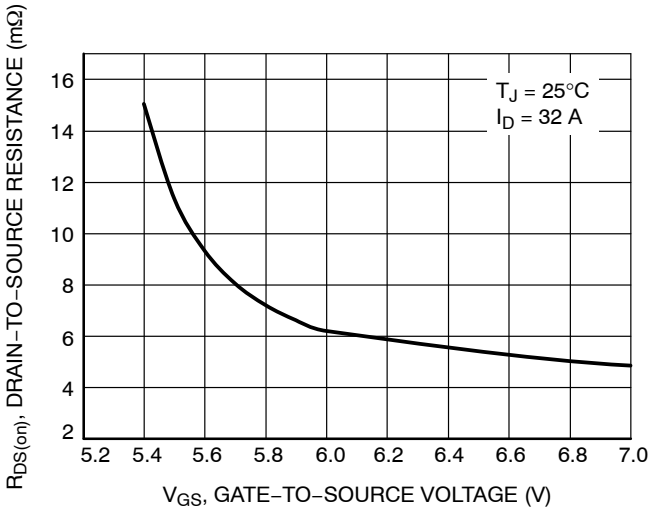


Figure 3. On−Resistance vs. Gate−to−Source Voltage

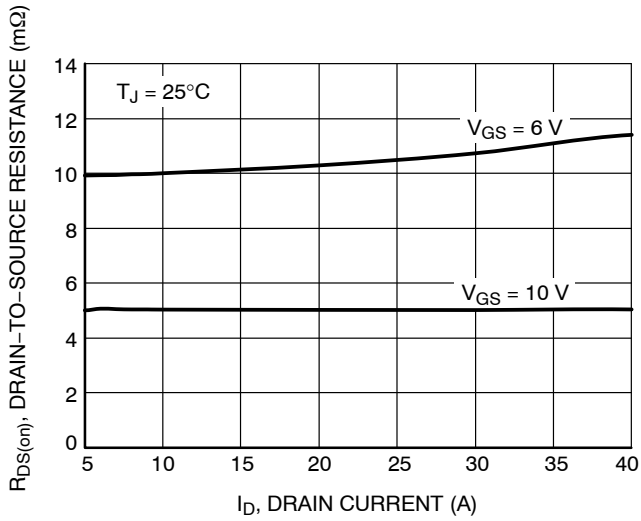


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

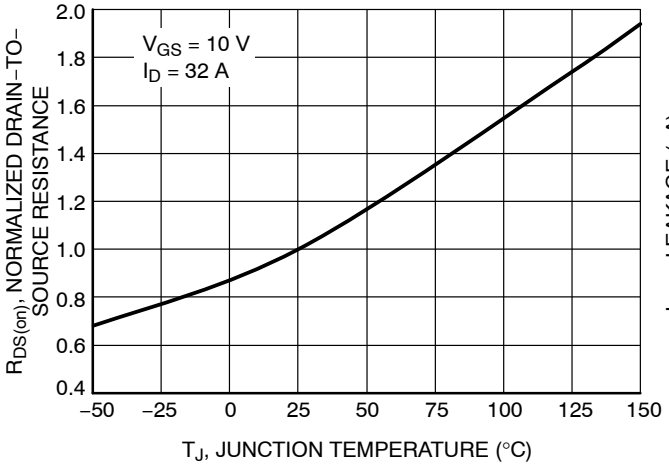


Figure 5. On−Resistance Variation with Temperature

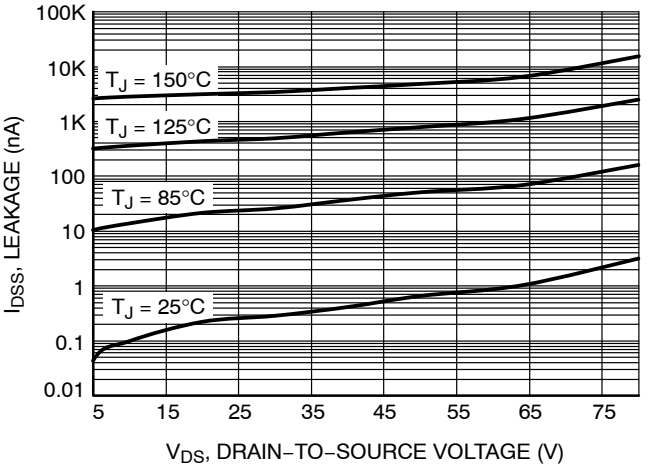


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

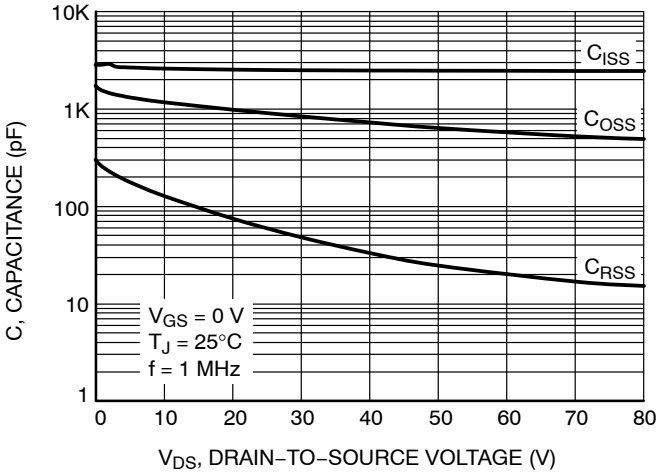


Figure 7. Capacitance Variation

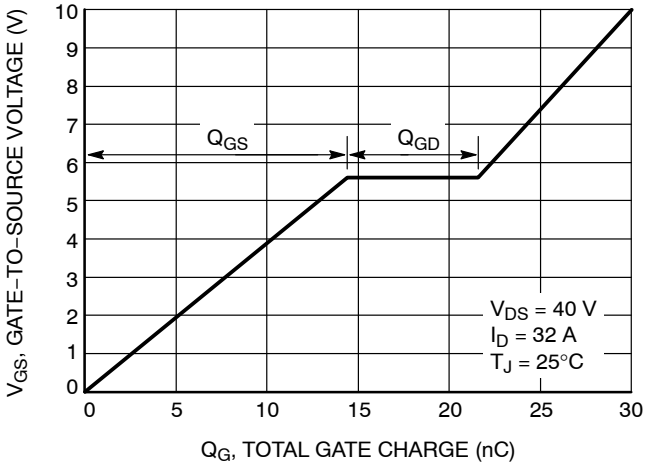


Figure 8. Gate−to−Source Voltage vs. Total Charge

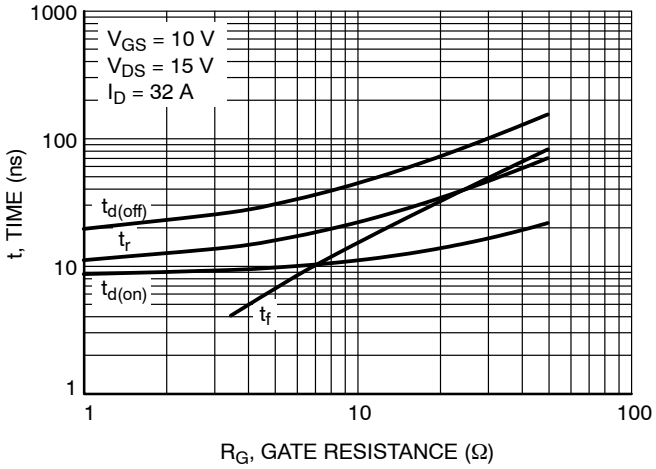


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

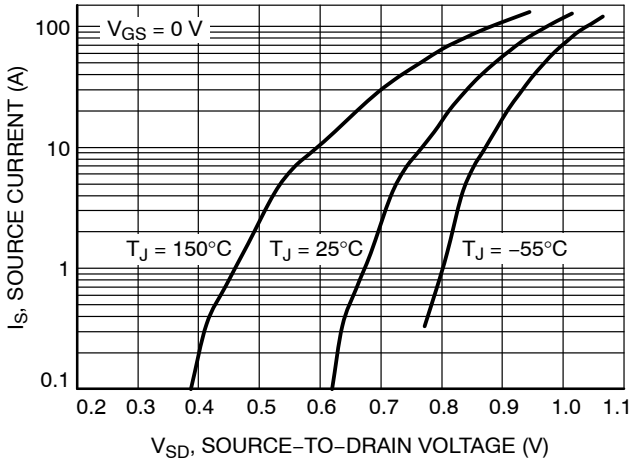


Figure 10. Diode Forward Voltage vs. Current

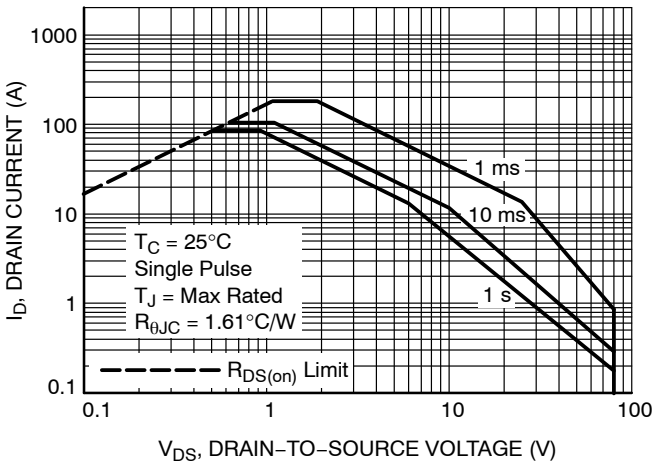


Figure 11. Safe Operating Area

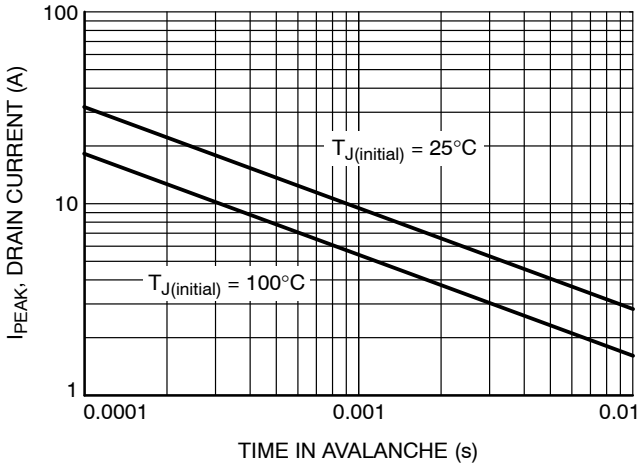


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

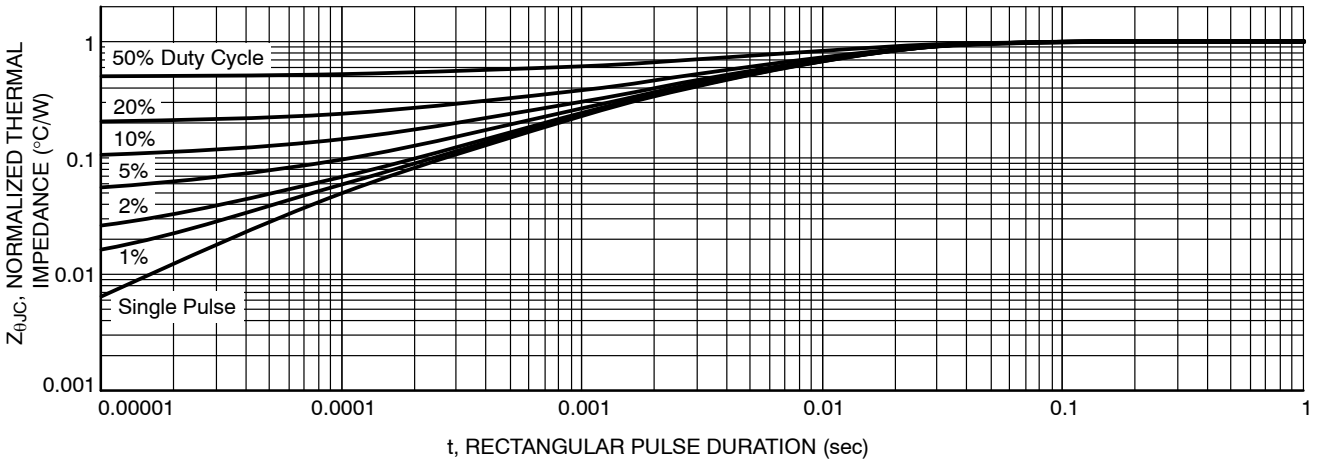


Figure 13. Transient Thermal Response

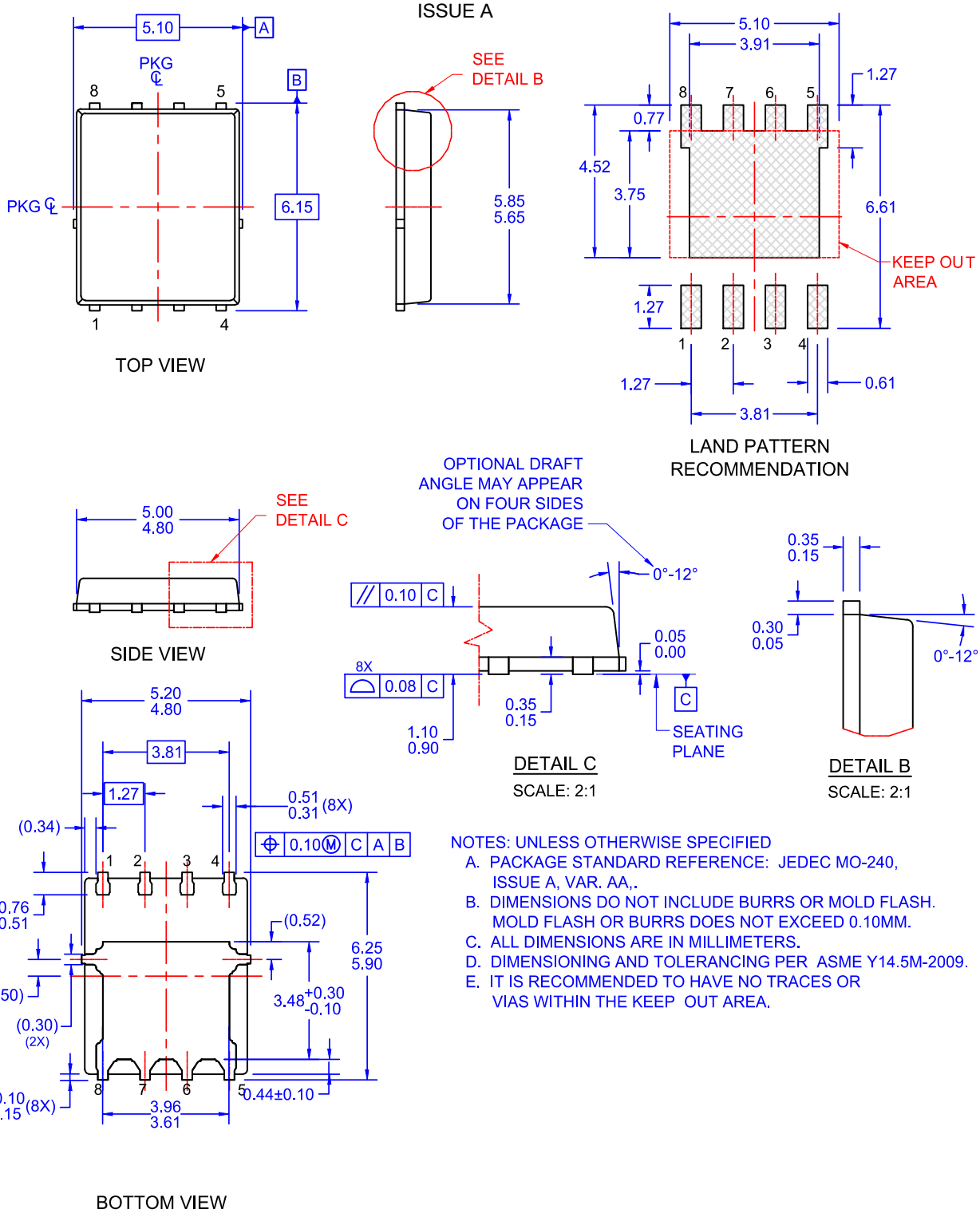
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS006N08MC	06N08	PQFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

PQFN8 5X6, 1.27P
CASE 483AE
ISSUE A



NOTES: UNLESS OTHERWISE SPECIFIED

A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

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North American Technical Support:
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