

# MOSFET - Power, Single N-Channel, PQFN8 80 V, 32 A



ON Semiconductor®

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## NTMFS006N08MC

### Features

- Advanced Package (5x6mm) with Excellent Thermal Conduction
- Ultra Low  $R_{DS(on)}$  to Improve System Efficiency
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Hot Swap Application
- Power Load Switch
- Battery Management and Protection

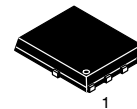
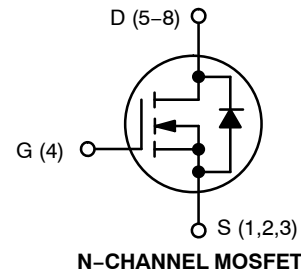
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DS}$	80	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$ 82	A
		$T_C = 85^\circ\text{C}$	59	
Power Dissipation $R_{\theta JC}$ (Note 3)	Steady State	$T_C = 25^\circ\text{C}$	$P_D$ 78	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ 14.7	A
		$T_A = 85^\circ\text{C}$	10.6	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 2.5	W
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ 9.3	A
		$T_A = 85^\circ\text{C}$	6.7	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 1.0	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$ 216	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_L = 32 A_{pk}$ )		$E_{AS}$ 51	mJ	
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

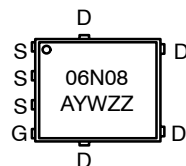
1. Surface-mounted on FR4 board using 1 in<sup>2</sup> pad, 2 oz Cu pad.
2. Surface-mounted on FR4 board using minimum pad size, 2 oz Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
80 V	6.0 m $\Omega$ @ 10 V	32 A
80 V	17 m $\Omega$ @ 6 V	16 A



PQFN8  
T1 SUFFIX  
CASE 483AE

### MARKING DIAGRAMS



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NTMFS006N08MC

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	1.61	°C/W
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	50	
Junction-to-Ambient – Steady State (Note 5)	$R_{\theta JA}$	125	

4. Surface-mounted on FR4 board using 1 in<sup>2</sup> pad, 2 oz Cu pad.  
 5. Surface-mounted on FR4 board using minimum pad size, 2 oz Cu pad.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		96.6		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 64\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

### ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.0		4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 200\ \mu\text{A}$ , ref to $25^\circ\text{C}$		-5		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 32\text{ A}$		4.9	6.0	m $\Omega$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 6\text{ V}, I_D = 16\text{ A}$		10.2	17	m $\Omega$
Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$		0.3		$\Omega$

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$		2300		pF
Output Capacitance	$C_{OSS}$			710		
Reverse Transfer Capacitance	$C_{RSS}$			31		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}; I_D = 32\text{ A}$		30		nC
Threshold Gate Charge	$Q_{G(TH)}$			3.3		
Gate-to-Source Charge	$Q_{GS}$			10		
Gate-to-Drain Charge	$Q_{GD}$			6.0		

### SWITCHING CHARACTERISTICS (Note 7)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 32\text{ A}, R_G = 2.5\ \Omega$		13		ns
Rise Time	$t_r$			4		
Turn-Off Delay Time	$t_{d(OFF)}$			18		
Fall Time	$t_f$			4		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 32\text{ A}$	$T_J = 25^\circ\text{C}$	0.84	1.2	V
			$T_J = 125^\circ\text{C}$	0.78		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 32\text{ A}$		49.58		ns
Reverse Recovery Charge	$Q_{RR}$			51.4		nC

6. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 7. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

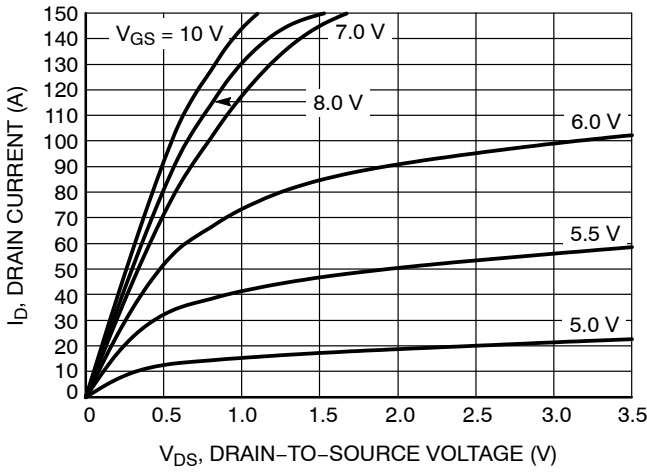


Figure 1. On-Region Characteristics

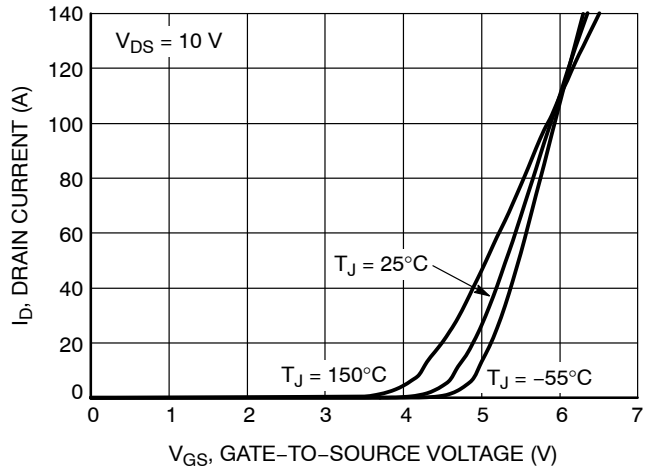


Figure 2. Transfer Characteristics

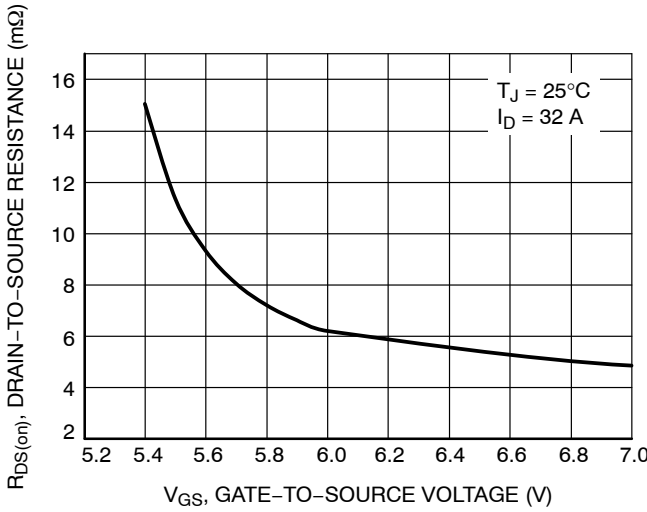


Figure 3. On-Resistance vs. Gate-to-Source Voltage

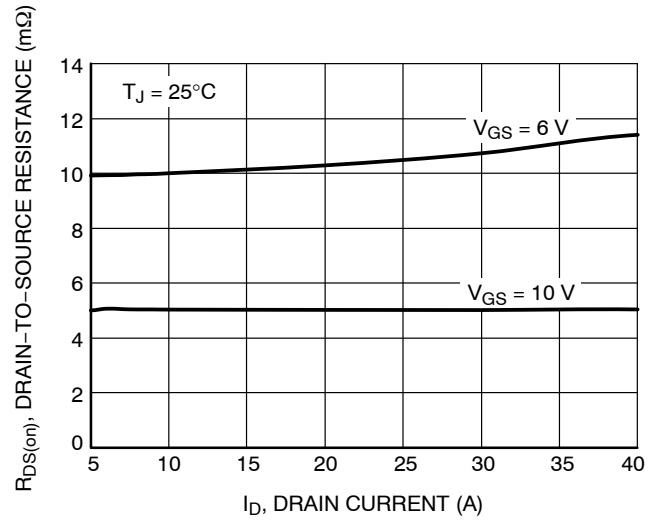


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

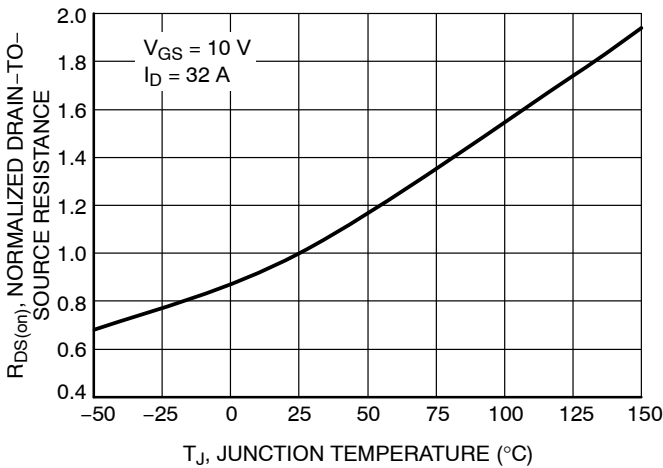


Figure 5. On-Resistance Variation with Temperature

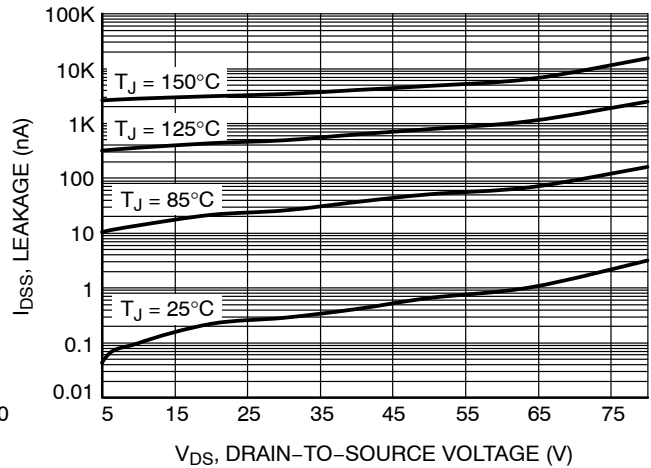


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTMFS006N08MC

## TYPICAL CHARACTERISTICS

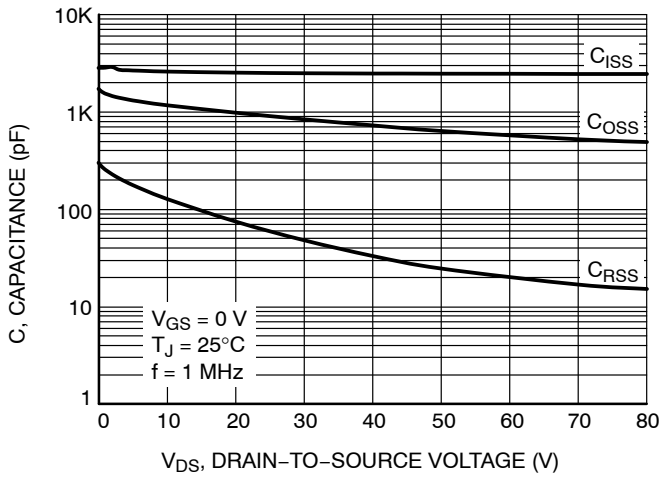


Figure 7. Capacitance Variation

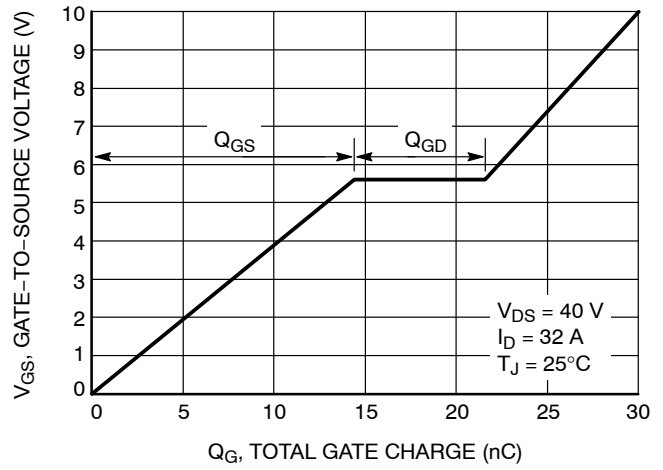


Figure 8. Gate-to-Source Voltage vs. Total Charge

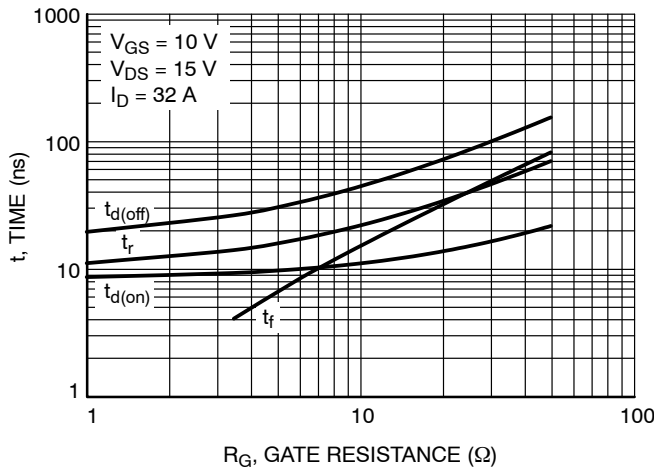


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

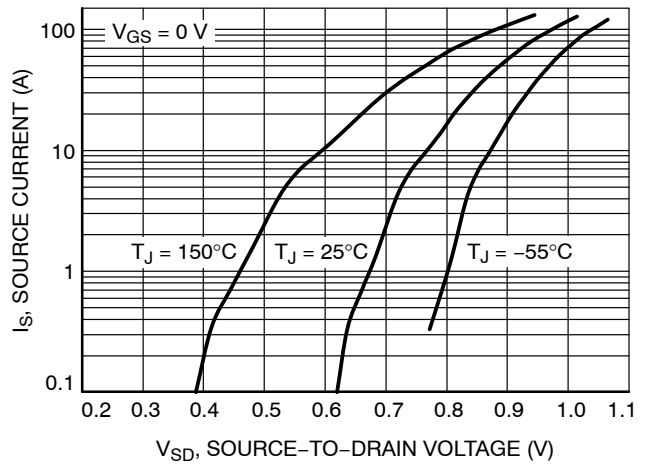


Figure 10. Diode Forward Voltage vs. Current

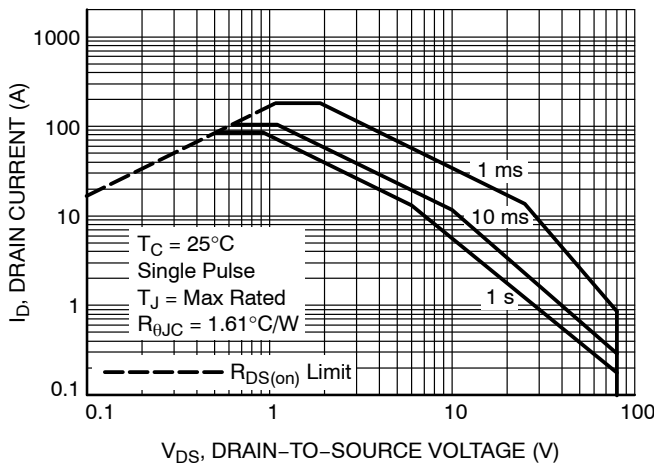


Figure 11. Safe Operating Area

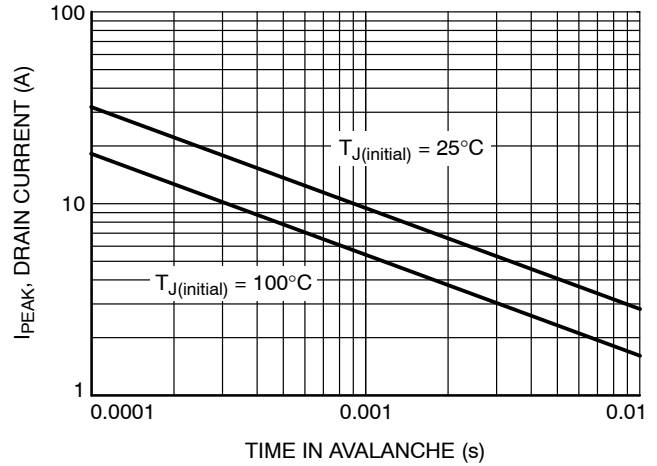
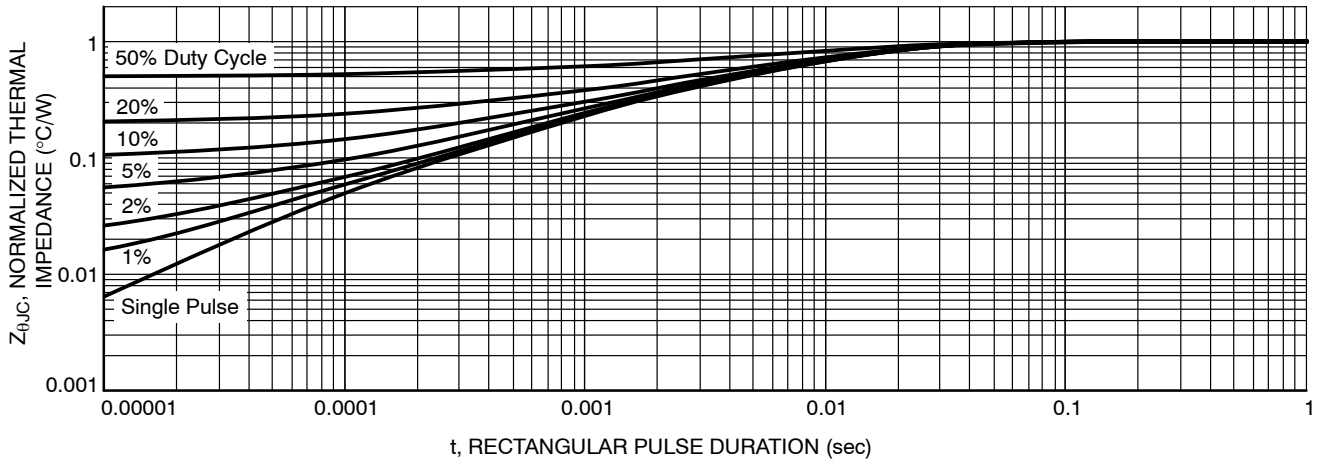


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NTMFS006N08MC

## TYPICAL CHARACTERISTICS



**Figure 13. Transient Thermal Response**

### DEVICE ORDERING INFORMATION

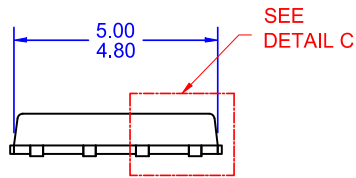
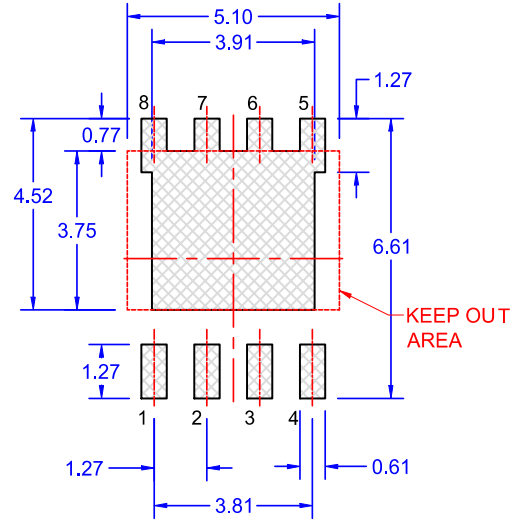
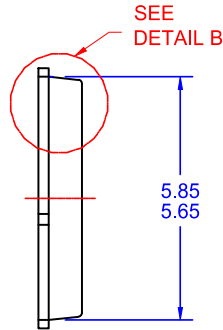
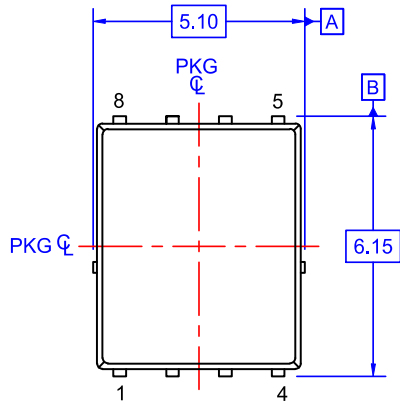
Device	Marking	Package	Shipping†
NTMFS006N08MC	06N08	PQFN8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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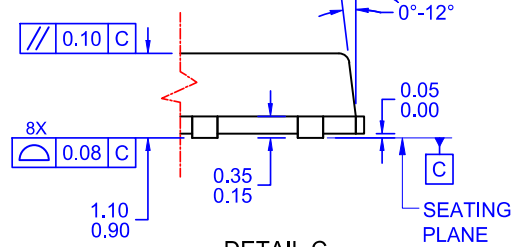
## PACKAGE DIMENSIONS

PQFN8 5X6, 1.27P  
CASE 483AE  
ISSUE A

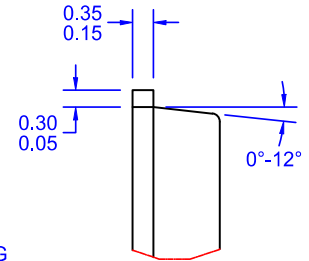


SIDE VIEW

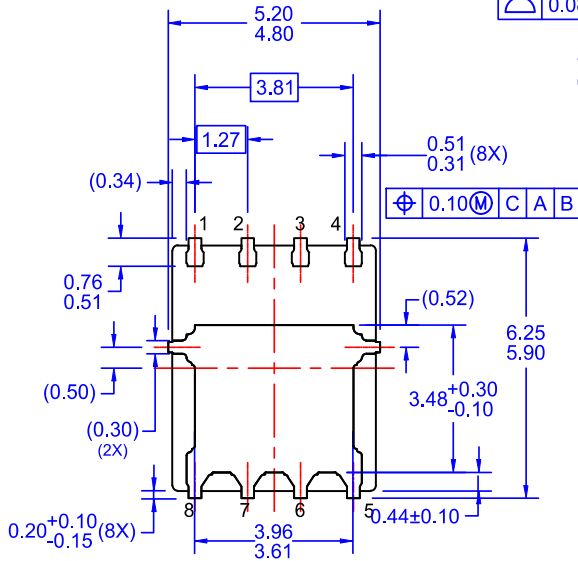
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



SCALE: 2:1




SCALE: 2:1



NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.,
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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