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NTE9664
Integrated Circuit
HTL – Master/Slave R/S Flip–Flop
14–Lead DIP

Description:

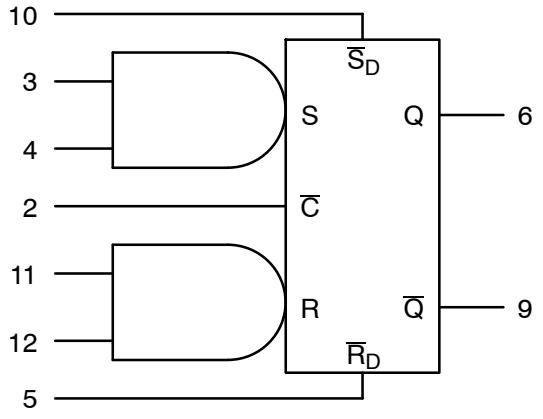
The NTE9664 is a DC coupled R/S flip–flop in a 14–Lead DIP type package operating on the master/slave principle. Information is entered in the master section while the clock pulse is high and is transferred to the slave when the clock goes negative.

Absolute Maximum Ratings: (T_A = +25°C unless otherwise specified)

Power Supply Voltage, V_{CC}
- Continuous 18V
- Pulsed (1.0s) 20V

Output Current (Into Outputs), I_O 26mA
Input Reverse Current (at 18V), I_R 0.5mA
Operating Temperature Range, T_A . . . . . –30° to +75°C
Storage Temperature Range, T_{stg} . . . . . –55° to +125°C

Logic Diagram



Input Loading Factor
- C Input = 3
- Other Inputs = 1

Output Loading Factor = 8

Loading factors are valid from –30° to +75°C
- with V_{CC} = 15 ±1Vdc

Ft_{og} = 3.0Mhz Typ

Total Power Dissipation = 160mW Typ

Electrical Characteristics: (T_A = +25°C unless otherwise specified)

									Test Current/Voltage Values (All Temperatures)											
									mA		Volts									
									I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}				
									9.6	–0.024	6.5	8.5	1.5	16	14	16				
Parameter	Symbol	Pin Under Test	Test Limits						Unit	Test Current/Voltage Applied to Pins Listed Below										
			–30°C		+25°C		+75°C													
			Min	Max	Min	Max	Min	Max		I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}	CP_a	CP_b	Ground
Output Voltage	V_{OL}	6*	–	1.5	–	1.5	–	1.5		6	–	–	3,4,11,12	–	–	14	–	–	5	7
		6	–	1.5	–	1.5	–	1.5	Vdc	6	–	4	3,5,11,12	–	–	14	–	2	–	7
		6	–	1.5	–	1.5	–	1.5	Vdc	6	–	3	4,5,11,12	–	–	14	–	2	–	7
		9Ŧ	–	1.5	–	1.5	–	1.5	Vdc	9	–	–	3,4,11,12	–	–	14	–	–	10	7
		9	–	1.5	–	1.5	–	1.5	Vdc	9	–	11	3,4,10,12	–	–	14	–	2	–	7
		9	–	1.5	–	1.5	–	1.5	Vdc	9	–	12	3,4,10,11	–	–	14	–	2	–	7
	V_{OH}	6	–	–	12.5	–	12.5	–	Vdc	–	6	–	5	–	–	14	–	–	–	2,3,4,7,10,11,12
		9	–	–	12.5	–	12.5	–	Vdc	–	9	–	10	–	–	14	–	–	–	2,3,4,5,7,11,12
Short–Circuit Current	I_{SC}	6	–	–	–6.5	–15	–6.5	–15	Vdc	–	–	2,5	10	–	–	–	14	–	–	6,7,9
		9	–	–	–6.5	–15	–6.5	–15	Vdc	–	–	2,10	9	–	–	–	14	–	–	6,7,9
Reverse Current	4 I_R	2§	–	–	–	8.0	–	8.0	µAdc	–	–	–	5	–	2	14	–	–	–	3,4,7,10,11,12
	4 I_R	2Ť	–	–	–	8.0	–	8.0	µAdc	–	–	–	10	–	2	14	–	–	–	3,4,5,7,11,12
	I_R	3	–	–	–	2.0	–	2.0	µAdc	–	–	–	–	–	3	14	–	–	–	2,4,7
		4	–	–	–	2.0	–	2.0	µAdc	–	–	–	–	–	4	14	–	–	–	2,3,7
		5	–	–	–	2.0	–	2.0	µAdc	–	–	–	2,11,12	–	5	14	–	–	–	7
		10	–	–	–	2.0	–	2.0	µAdc	–	–	–	2,3,4	–	10	14	–	–	–	7
		11	–	–	–	2.0	–	2.0	µAdc	–	–	–	–	–	11	14	–	–	–	2,7,12
		12	–	–	–	2.0	–	2.0	µAdc	–	–	–	–	–	12	14	–	–	–	2,7,11
Forward Current	3 I_F	2	–	–	–	–3.6	–	–3.6	mAdc	–	–	–	5	2	3,4,11,12	–	14	–	–	7,10
	3 I_F	2	–	–	–	–3.6	–	–3.6	mAdc	–	–	–	10	2	3,4,11,12	–	14	–	–	5,7
	I_F	3	–	–	–	–1.2	–	–1.2	mAdc	–	–	–	–	3	2,4	–	14	–	–	7
		4	–	–	–	–1.2	–	–1.2	mAdc	–	–	–	–	4	2,3	–	14	–	–	7
		5	–	–	–	–1.2	–	–1.2	mAdc	–	–	–	–	5	–	–	14	–	–	2,7,10,11,12
		10	–	–	–	–1.2	–	–1.2	mAdc	–	–	–	–	10	–	–	14	–	–	2,3,4,5,7
		11	–	–	–	–1.2	–	–1.2	mAdc	–	–	–	–	11	2,12	–	14	–	–	7
		12	–	–	–	–1.2	–	–1.2	mAdc	–	–	–	–	12	2,11	–	14	–	–	7
Power Drain Current	I_{CCL}	14	–	–	–	14.5	–	–	mAdc	–	–	–	–	–	–	–	14	–	–	2,3,4,5,7,10,11,12
	I_{CCH}	14	–	–	–	14.5	–	–	mAdc	–	–	–	–	–	–	–	14	–	–	7

Note 1. Pins not listed are left open.

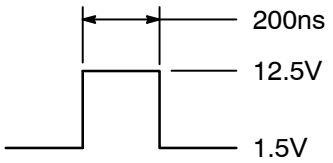
* Apply momentary ground to Pin9 and Pin10 prior to clock pulse.

Ŧ Apply momentary ground to Pin5 and Pin6 prior to clock pulse.

§ Apply momentary ground to Pin9.

Ť Apply momentary ground to Pin6.

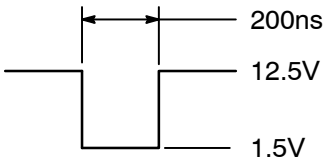
CP_a



$t_r \leq 1.0\mu s$ (10% to 90%)

$t_f \leq 1.0\mu s$ (90% to 10%)

CP_b



$t_r \leq 1.0\mu s$ (10% to 90%)

$t_f \leq 1.0\mu s$ (90% to 10%)

Truth Tables:

Direct Input Operation:

$\overline{R}_D$	$\overline{S}_D$	Q	$\overline{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

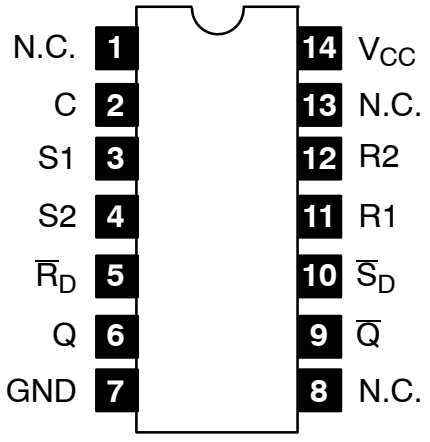
NC = No change
NA = Not allowed

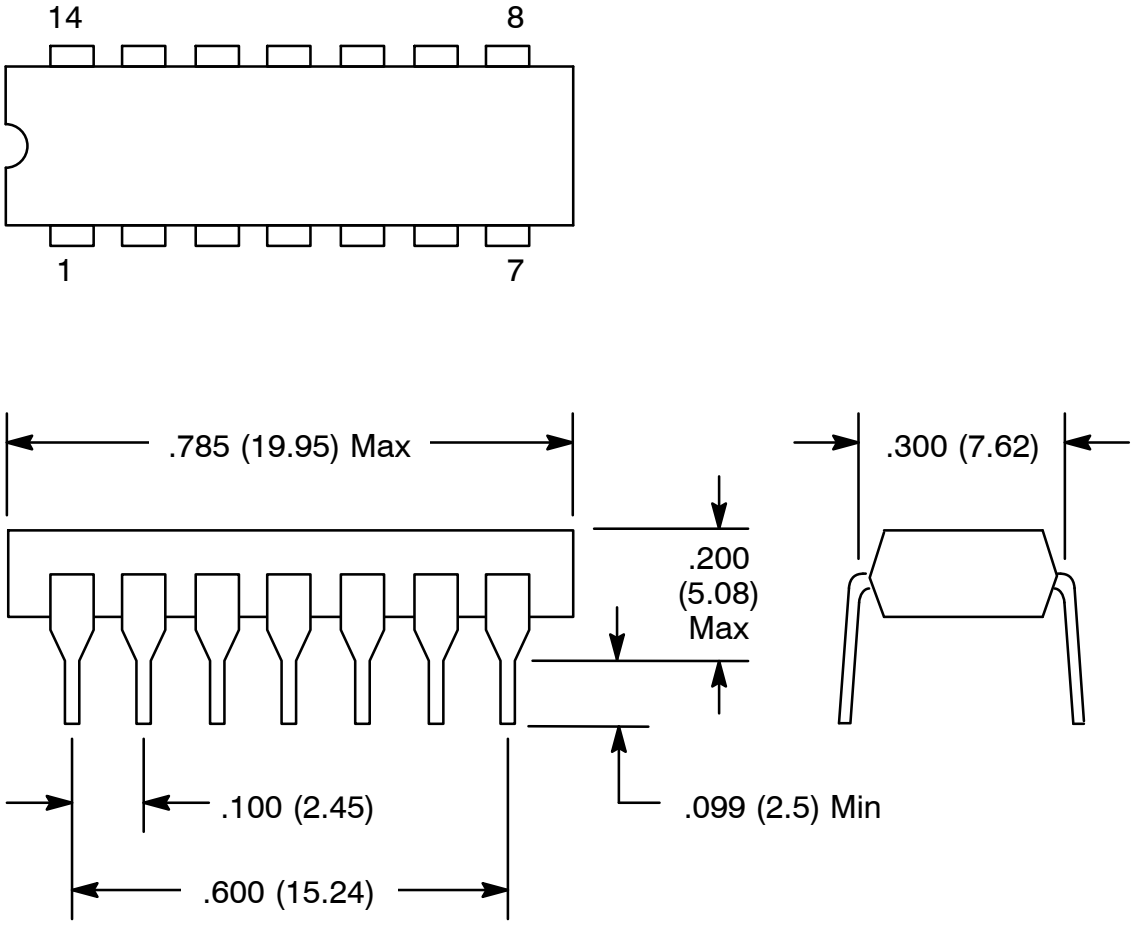
Clocked Operation:

t_n				$T_n + 1$
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	0

Direct inputs ($\overline{R}_D$, $\overline{S}_D$) must be high.
0 = low state
1 = high state
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
$t_n + 1$ = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

Pin Connection Diagram




14
8
1
7
.785 (19.95) Max
.300 (7.62)
.200
(5.08)
Max
.100 (2.45)
.099 (2.5) Min
.600 (15.24)