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NTE8308
Integrated Circuit
Transistor Transistor Logic (TTL)
Dual 4–Bit Latch

Description:

The NTE8308 is a dual 4–bit D–type latch in a 24–Lead DIP type plastic package designed for general purpose storage applications in digital systems. Each latch contains both an active LOW Master Reset input an active LOW Enable inputs.

Data can be entered into the NTE8308 latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input. The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the Master Reset input.

Recommended Operating Conditions:

Supply Voltage, V_{CC} . . . . . 5V ±5%
Operating Temperature Range, T_{opr} . . . . . 0° to +70°C

Input Loading/Fan–Out:

Description	Pin Names	High	Low
Parallel Latch Inputs	$D_{0a} - D_{3a}$, $D_{0b} - D_{3b}$	1.5	1.5
AND Enable Inputs (Active LOW)	$\overline{E}_{0a1}$, $\overline{E}_{1a}$, $\overline{E}_{0b}$, $\overline{E}_{1b}$	1.0	1.0
Master Reset Inputs (Active LOW)	$\overline{MR}_a$, $\overline{MR}_b$	1.0	1.0
Parallel Latch Outputs	$Q_{0a} - Q_{3a}$, $Q_{0b} - Q_{3b}$	20	10

DC Characteristics: (T_A = 0° to +70°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Current	I_{CC}	V_{CC} = Max	–	–	100	mA

AC Characteristics: (V_{CC} = +5V, T_A = +25°C, C_L = 15pF, R_L = 400Ω)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay $\overline{E}_n$ to Q_n	t_{PLH}		–	–	30	ns
	t_{PHL}		–	–	22	ns
Propagation Delay D_n to Q_n	t_{PLH}		–	–	15	ns
	t_{PHL}		–	–	18	ns
Propagation Delay $\overline{MR}$ to Q_n	t_{PHL}		–	–	22	ns

AC Operating Requirements: (V_{CC} = +5V, T_A = +25°C)

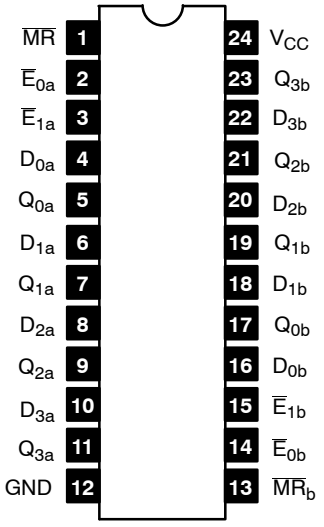
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Setup Time HIGH, D_n to $\overline{E}_n$	t_s (H)		10	–	–	ns
Hold Time HIGH, D_n to $\overline{E}_n$	t_h (H)		–2.0	–	–	ns
Setup Time LOW, D_n to $\overline{E}_n$	t_s (L)		12	–	–	ns
Hold Time LOW, D_n to $\overline{E}_n$	t_s (L)		8.0	–	–	ns
$\overline{E}_n$ Pulse Width LOW	t_w (L)		18	–	–	ns
$\overline{MR}$ Pulse Width LOW	t_w (L)		18	–	–	ns
Recovery Time, $\overline{MR}$ to $\overline{E}_n$	t_{rec}		8.0	–	–	ns

Truth Table:

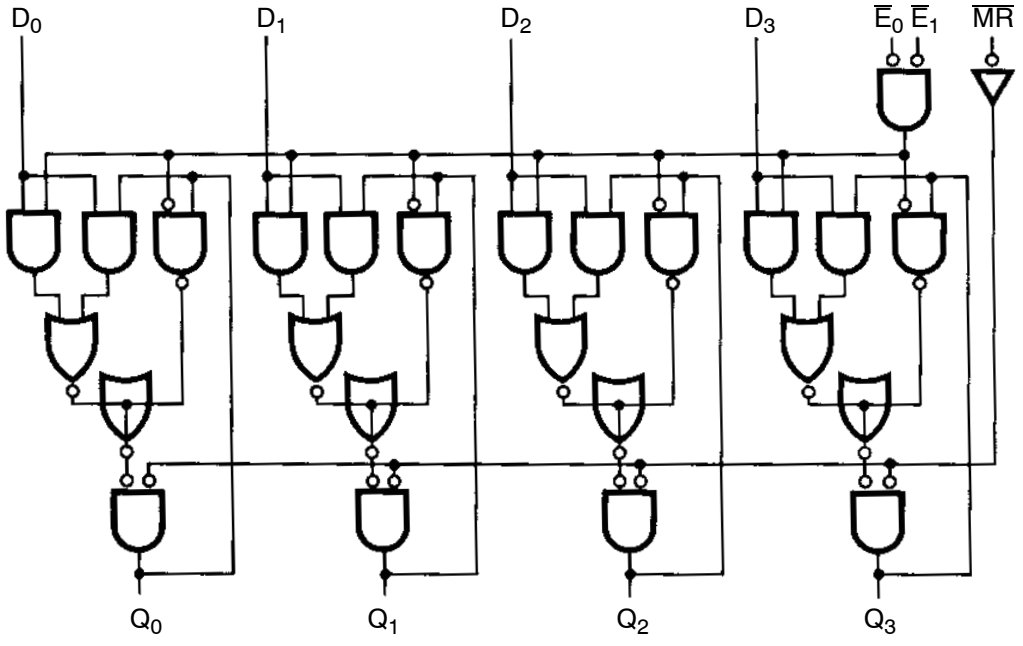
$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	D	Q_n	Operation
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

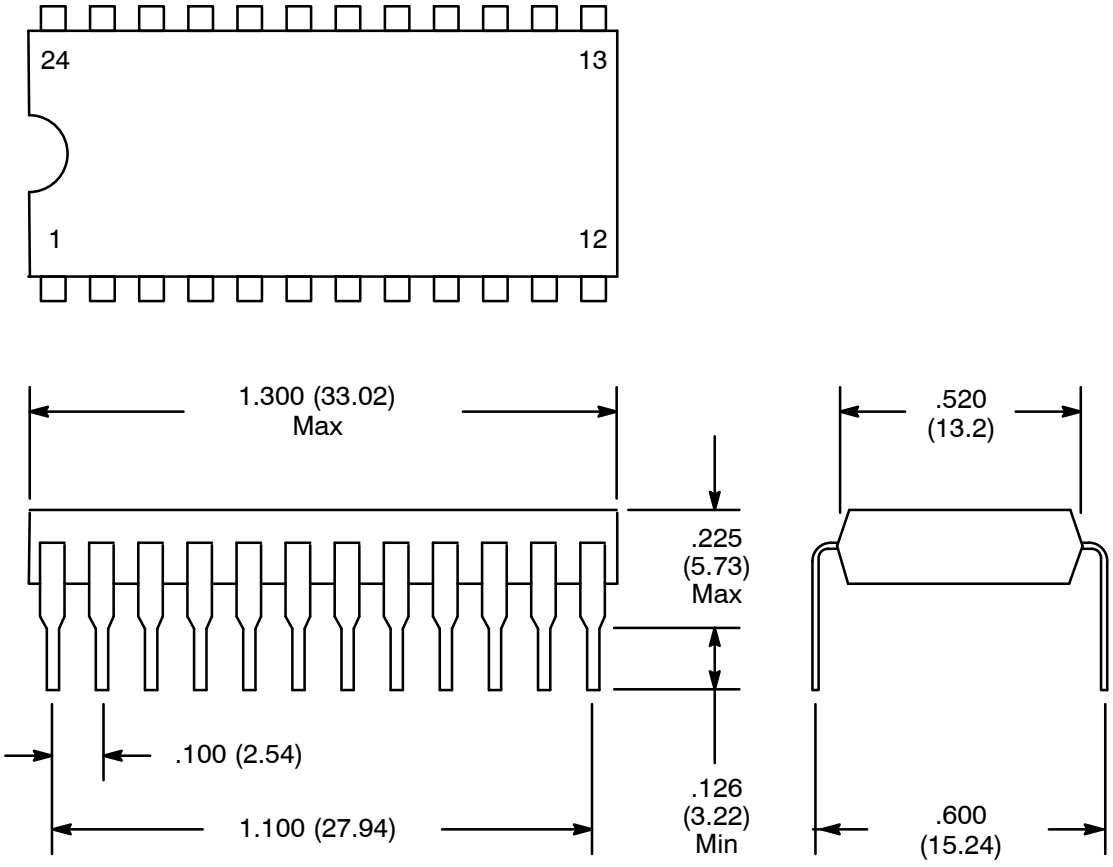
Q_{n-1} = Previuos Output Stage
Q_n = Present Output Stage
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Pin Connection Diagram



Logic Diagram




24
13
1
12
1.300 (33.02)
Max
.225
(5.73)
Max
.100 (2.54)
1.100 (27.94)
.126
(3.22)
Min
.520
(13.2)
.600
(15.24)