ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE80C95, NTE80C96, NTE80C97
Integrated Circuit
TTL, CMOS, TRI–STATE Hex Buffers

Description:

These gates are monolithic complementary MOS (CMOS) integrated circuits in a 16–Lead DIP type package constructed with N– and P–channel enhancement mode transistors. These devices convert CMOS or TTL outputs to TRI–STATE outputs with no logic inversion, the NTE80C96 and the NTE80C98 provide the logical opposite of the input signal. The NTE80C95 and the NTE80C96 have common TRI–STATE controls for all six devices. The NTE80C97 and the NTE80C98 have two TRI–STATE controls; one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features:

- Wide Supply Voltage Range: 3.0V to 15V
- Guaranteed Noise Margin: 1.0V
- High Noise Immunity: 0.45 V_{CC} (typ)
- TTL Compatible: Drive 1 TTL Load
- Typical Propagation Delay: 40ns into 150pF Load

Applications:

- Bus Drivers

Absolute Maximum Ratings: (Note 2)

Voltage at any Pin . . . . . –0.3V to V_{CC} + 0.3V
Operating Temperature Range . . . . . –40° to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Package Dissipation 500mW
Power Supply Voltage (V_{CC}) 18V
Lead Temperature (During Soldering, 10sec Max) . . . . . +300°C

Note 1. **NTE80C95** is a **discontinued** device and **no longer available**.

Note 2. ”Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for ”Operating Temperature Range” they are not meant to imply that the devices should be operated at these limits. The table of ”Electrical Characteristics” provides conditions for actual device operation.

DC Electrical Characteristics: (Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
CMOS to CMOS							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 5V		3.5	–	–	V
		V_{CC} = 10V		8.0	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 5V		–	–	1.5	V
		V_{CC} = 10V		–	–	2.0	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 5V		4.5	–	–	V
		V_{CC} = 10V		9.0	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 5V		–	–	0.5	V
		V_{CC} = 10V		–	–	1.0	V
Logical “1” Input Current	$I_{IN(1)}$	V_{CC} = 15V		–	0.005	1.0	μA
Logical “0” Input Current	$I_{IN(0)}$			–1.0	–0.005	–	μA
Output Current in High Impedance State	I_{OZ}	V_{CC} = 15V	V_O = 15V	–	0.005	1.0	μA
			V_O = 0V	–1.0	–0.005	–	μA
Supply Current	I_{CC}	V_{CC} = 15V		–	0.01	15	μA
TTL Interface							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 4.75V		V_{CC}–1.5	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 4.75V		–	–	0.8	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 4.75V, I_O = –1.6mA		2.4	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 4.75V, I_O = –1.6mA		–	–	0.4	V
Output Drive (Short–Circuit Current)							
Output Source Current	I_{SOURCE}	V_{CC} = 5V, $V_{IN(1)}$ = 5V	T_A = +25°C, V_{OUT} = 0V	–4.35	–	–	mA
		V_{CC} = 10V, $V_{IN(1)}$ = 10V		–20	–	–	mA
Output Sink Current	I_{SINK}	V_{CC} = 5V, $V_{IN(0)}$ = 5V	T_A = +25°C, V_{OUT} = V_{CC}	4.35	–	–	mA
		V_{CC} = 10V, $V_{IN(0)}$ = 10V		20	–	–	mA

Note 3. Max/Min Limits apply across temperature range, unless otherwise noted.

AC Electrical Characteristics: (T_A = +25°C, C_L = 50pF, Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Propagation Delay Time to a Logical “0” or Logical “1” from Data Input to Output NTE80C95, NTE80C97	t_{pd0}, t_{pd1}	V_{CC} = 5V		–	60	100	ns
		V_{CC} = 10V		–	25	40	ns
NTE80C96		V_{CC} = 5V		–	70	150	ns
		V_{CC} = 10V		–	35	75	ns
Propagation Delay Time to a Logical “0” or Logical “1” from Data Input to Output NTE80C95, NTE80C97	t_{pd0}, t_{pd1}	C_L = 150pF	V_{CC} = 5V	–	85	160	ns
			V_{CC} = 10V	–	40	80	ns
NTE80C96			V_{CC} = 5V	–	95	210	ns
			V_{CC} = 10V	–	45	110	ns

Note 4. AC parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Cont'd): (T_A = +25°C, C_L = 50pF, Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Delay from Disable Input to High Impedance State (from Logical "1" or Logical "0") NTE80C95	t_{1H}, t_{0H}	R_L = 10k, C_L = 5pF	V_{CC} = 5V	–	80	135	ns
			V_{CC} = 10	–	50	90	ns
NTE80C96			V_{CC} = 5V	–	100	180	ns
			V_{CC} = 10V	–	70	125	ns
NTE80C97			V_{CC} = 5V	–	70	125	ns
			V_{CC} = 10V	–	50	90	ns
Delay from Disable Input to Logical "1" (from High Impedance State) NTE80C95	t_{H1}, t_{H0}	R_L = 10k, C_L = 5pF	V_{CC} = 5V	–	120	200	ns
			V_{CC} = 10	–	50	90	ns
NTE80C96			V_{CC} = 5V	–	130	225	ns
			V_{CC} = 10V	–	60	110	ns
NTE80C97			V_{CC} = 5V	–	95	175	ns
			V_{CC} = 10V	–	40	80	ns
Input Capacitance	C_{IN}	Any Input, Note 5		–	5	–	pF
Output Capacitance TRI–STATE	C_{OUT}	Any Output, Note 5		–	11	–	pF
Power Dissipation Capacitance	C_{PD}	Note 6		–	60	–	pF

Note 4. AC parameters are guaranteed by DC correlated testing.
Note 5. Capacitance is guaranteed by periodic testing.
Note 6. C_{PD} determines the no load AC power consumption of any CMOS device.

Truth Table (NTE80C95, NTE80C96):

Disable DIS_1	Input DIS_2	Input	Output
0	0	0	0
0	0	1	1
0	1	X	H–z
1	0	X	H–z
1	1	X	H–z

Truth Table (NTE80C97):

Disable DIS_4	Input DIS_2	Input	Output
0	0	0	0
0	0	1	1
X	1	X	H–z *
1	X	X	H–z **

* Output 5–6 Only
** Output 1–4 Only
X = Don't Care

Pin Connection Diagram