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NTE74LS290
Integrated Circuit
TTL – Decade Counter (Divide by 2 & 5)

Description:

The NTE74LS290 is a monolithic counter in a 14–Lead plastic DIP type package that contains four master–slave flip–flops and additional gating to provide a divide–by–two counter and a three–stage binary counter for which the count cycle length is divide–by five.

The NTE74LS290 has a gated zero reset and also contains gated set–to–nine inputs for use in BCD nine's complement applications.

To use the maximum count length, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide–by–ten count can be obtained by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide–by–ten square wave at output Q_A.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN}
R Inputs 7V
A and B Inputs 5.5V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Output Current	I_{OH}	–	–	–400	μA
Low–Level Output Current	I_{OL}	–	–	8	mA
Count Frequency A Input	f_{count}	0	–	32	MHz
B Input		0	–	16	MHz
Pulse Width A Input	t_w	15	–	–	ns
B Input		30	–	–	ns
Reset Inputs		30	–	–	ns
Reset Inactive–State Setup Time	t_{su}	25	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}			2	–	–	V
Low Level Input Voltage	V_{IL}			–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = –18mA		–	–	–1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = –400μA		2.7	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA, Note 4	–	0.25	0.4	V
			I_{OL} = 8mA, Note 4	–	0.35	0.5	V
Input Current Any Reset	I_I	V_{CC} = MAX, V_I = 7V		–	–	0.1	mA
A Input		V_{CC} = MAX, V_I = 5.5V		–	–	0.2	mA
B Input				–	–	0.4	mA
High Level Input Current Any Reset	I_{IH}	V_{CC} = MAX, V_I = 2.7V		–	–	20	μA
A Input				–	–	40	μA
B Input				–	–	80	μA
Low Level Input Current Any Reset	I_{IL}	V_{CC} = MAX, V_I = 0.4V		–	–	–0.4	mA
A Input				–	–	–2.4	mA
B Input				–	–	–3.2	mA
Short–Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 5		–20	–	–100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 6		–	9	15	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Q_A outputs are tested at specified I_{OL} plus the ,limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan–out capability.

Note 5. Not more than one output should be shorted at a time, and the duration of the short–circuit should not exceed one second.

Note 6. I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Count Frequency (From A Input to Q_A Output)	f_{max}	R_L = 2kΩ, C_L = 15pF	32	42	–	MHz
(From B Input to Q_B Output)			16	–	–	MHz
Propagation Delay Time (From A Input to Q_A Output)	t_{PLH}		–	10	16	ns
	t_{PHL}		–	12	18	ns
Propagation Delay Time (From A Input to Q_D Output)	t_{PLH}		–	32	48	ns
	t_{PHL}		–	34	50	ns
Propagation Delay Time (From B Input to Q_B Output)	t_{PLH}		–	10	16	ns
	t_{PHL}		–	14	21	ns
Propagation Delay Time (From B Input to Q_C Output)	t_{PLH}		–	21	32	ns
	t_{PHL}		–	23	35	ns
Propagation Delay Time (From B Input to Q_D Output)	t_{PLH}		–	21	32	ns
	t_{PHL}		–	23	35	ns

Switching Characteristics (Cont'): (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From Set−to−0 Input to Any Output)	t_{PHL}	R_L = 2kΩ, C_L = 15pF	−	26	40	ns
Propagation Delay Time (From Set−to−9 Input to Q_A, Q_D Output)	t_{PLH}		−	20	30	ns
(From Set−to−9 Input to Q_B, Q_C Output)	t_{PHL}		−	26	40	ns

BCD Count Sequence: (Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi−Quinary (5−2): (Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = High Level
L = Low Level
X = Irrelevant

Note A: Output Q_A is connected to input B for BCD count.
Note B: Output Q_D is connected to input A for bi−quinary count.

Reset/Count Function Table:

Reset Inputs				Outputs			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = High Level, L = Low Level, X = Irrelevant

Pin Connection Diagram