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NTE74LS175
Integrated Circuit
TTL – Quad D–Type Flip–Flop with Clear

Description:

The NTE74LS175 is a monolithic, positive–edge–triggered flip–flop in a 16–Lead plastic DIP type package that utilizes TTL circuitry to implement D–type flip–flop logic. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive–going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive–going pulse. When the clock input is at either the high or low level, the D input signal ha no effect at the output.

Features:

- Contains Four Flip–Flops with Double Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip–Flop

Applications:

- Buffer/Storage Register
- Shift Register
- Pattern Generator

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 7V
Power Dissipation 14mW
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	−400	μA
Low−Level Output Current	I_{OL}	–	–	8	mA
Clock Frequency	f_{clock}	0	–	30	MHz
Width of Clock or Clear Pulse	t_w	20	–	–	ns
Setup Time Data Input	t_{su}	20	–	–	ns
Clear Inactive State		25	–	–	ns
Data Hold Time	t_h	5	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}			2	–	–	V
Low−Level Input Voltage	V_{IL}			–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA		–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = −400μA		2.7	3.5	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	–	0.25	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 7V		–	–	0.1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V		–	–	20	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V		–	–	−0.4	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4		−20	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5		–	11	18	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time, and duration of the short−circuit should not exceed one second.

Note 5. With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 2kΩ, C_L = 15pF	30	40	–	MHz
Propagation Delay Time, from Clear Input	t_{PLH}		–	20	30	ns
	t_{PHL}		–	20	30	ns
Propagation Delay Time, from Clock Input	t_{PLH}		–	13	25	ns
	t_{PHL}		–	16	25	ns

Function Table (Each Flip–Flop):

Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	**$\overline{Q}$**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_o	$\overline{Q}_o$

H = HIGH Level (Steady State)
L = LOW Level (Steady State)
X = Irrelevant
↑ = Transition from LOW to HIGH Level
Q_0 = The level of Q before the indicated steady state input conditions were established

Pin Connection Diagram