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NTE74LS170
Integrated Circuit
TTL – 4–by–4–Register File with Open Collector Outputs

Description:

The NTE74LS170 is a 4–by–4 register with open collector outputs in a 16–Lead plastic DIP type package incorporating the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on–chip decoding is provided for addressing th four word locations to either write–in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4–bit word to be stored. Location of the word is determined by the write–address inputs A and B in conjunction with a write–enable signal. Data applied at he inputs should be in its true form. That is, if a high–level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at th D input is transferred to the latch output. When the write–enable input, $\overline{G}_W$, is high, the data inputs are inhibited and heir levels can cause no change in the information stored in the internal latches. When the read–enable input, $\overline{G}_R$, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read–enable signal, the word appears at the four outputs.

This arrangement — data–entry addressing separate from data–read addressing and individual sense line — eliminates recovery times, permits simultaneous reading an writing, an is limited in speed only by the write time (30 nanoseconds typical) and the read time (25 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except the read enable and write enable are buffered to lower the drive requirements to one LS–TTL standard load. Input–clamping diodes minimize switching transients to simplify system design. High=speed, double–ended AND–OR–INVERT gates are employed for the read–address function and drive high–sink–current, open–collector outputs. Up to 256 of these outputs may be wired–AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n–bit word length.

Features:

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Time: 20ns (Typ)
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n–Bits

Applications:

- Scratch–Pad Memory
- Buffer Storage between Processors
- Bit Storage in Fast Multiplication Designs

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 7V
Off−State Output Voltage 7V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . −65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Voltage	V_{OH}	–	–	5.5	V
Low−Level Output Current	I_{OL}	–	–	8	mA
Width of Write−Enable or Read−Enable Pulse	t_w	25	–	–	ns
Setup Times, High−Level or Low−Level Data Data Input with respect to Write Enable	$t_{su(D)}$	10	–	–	ns
Write Select with respect to Write Enable	$t_{su(W)}$	15	–	–	ns
Hold Times, High−Level or Low−Level Data (Note 2) Data Input with respect to Write Enable	$t_{h(D)}$	15	–	–	ns
Write Select with respect to Write Enable	$t_{h(W)}$	5	–	–	ns
Latch Time for New Data (Note 3)	t_{latch}	25	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Note 2. Write−select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su(W)}$ can be ignored as any address selection sustained for the final 30ns of the write−enable pulse and during $t_{h(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

Note 3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

Electrical Characteristics: (Note 4, Note 5)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}			2	–	–	V
Low−Level Input Voltage	V_{IL}			–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA		–	–	−1.5	V
High Level Output Current	I_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, V_{OH} = 5.5V		–	–	100	μA
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	–	0.25	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 7V	Any D, R or W	–	–	0.1	mA
			$\overline{G}_R$ or $\overline{G}_W$	–	–	0.2	mA

Note 4. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 5. All typical values are at V_{CC} = 5V, T_A = +25°C.

Electrical Characteristics (Cont'd): (Note 4, Note 5)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V	Any D, R or W	–	–	20	μA
			$\overline{G}_R$ or $\overline{G}_W$	–	–	40	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	Any D, R or W	–	–	–0.4	mA
			$\overline{G}_R$ or $\overline{G}_W$	–	–	–0.8	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 6		–	25	40	mA

Note 4. .For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 5. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 6. I_{CC} is measured under the following worst−case conditions: 4.5V is applied to all data inputs and both enable inputs, all address inputs to GND, and all outputs are open.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From Read Enable Input to Any Q Output)	t_{PLH}	R_L = 2kΩ, C_L = 15pF	–	20	30	ns
	t_{PHL}		–	20	30	ns
Propagation Delay Time (From Read Select Input to Any Q Output)	t_{PLH}		–	25	40	ns
	t_{PHL}		–	24	40	ns
Propagation Delay Time (From Write Enable Input to Any Q Output)	t_{PLH}		–	30	45	ns
	t_{PHL}		–	26	40	ns
Propagation Delay Time (From Data Input to Any Q Output)	t_{PLH}		–	30	45	ns
	t_{PHL}		–	22	35	ns

Write Function Table:

Write Inputs			Word			
W_B	W_A	$\overline{G}_W$	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

Read Function Table:

Read Inputs			Word			
R_B	R_A	$\overline{G}_R$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

H = HIGH Level
L = LOW Level
X = Irrelevant
(Q = D) = The four selected internal flip−flop outputs will assume the state applied to the four external data inputs
Q_0 = The level of Q before the indicated input conditions were established
W0B1 = The first bit of word 0, etc.

Pin Connection Diagram