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NTE74HCT374
Integrated Circuit
TTL − High Speed CMOS,
Octal D−Type Flip−Flop with 3−State Outputs,
Common Output Control & Common Clock

Description:

The NTE74HCT374 is an octal D−type flip−flop in a 20−Lead DIP type package that uses advanced silicon−gate CMOS technology, which provides the inherent benefits of low power consumption and wide power supply range, but are LS−TTL input and output characteristic and pin−out compatible. The 3−STATE outputs are capable of driving 15 LS−TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and GND.

The NTE74HCT374 is a positive edge triggered flip−flop. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

NTE74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These devices are also plug−in replacements to LS−TTL devices and can be used to reduce power consumption in existing designs.

Features:

- TTL Input Characteristic Compatible
- Typical Propagation Delay: 20ns
- Low Input Current: 1µA (max)
- Low Quiescent Current: 80µA (max)
- Compatible with Bus−Oriented Systems
- High Output Drive Capability: 15 LS−TTL Loads

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC}	−0.5 to +7.0V
DC Input Voltage, V_{IN}	−1.5 to V_{CC} +1.5V
DC Output Voltage, V_{OUT}	−0.5 to V_{CC} + 0.5V
Clamp Diode Current, I_{IK}, I_{OK}	±20mA
DC Output Current (Per Pin), I_{OUT}	±35mA
DC V_{CC} or GND Current (Per Pin), I_{CC}	±70mA
Power Dissipation (Note 3), P_D	600mW
Storage Temperature Range, T_{stg}	−65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L	+260°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.
Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	–	5.5	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C
Input Rise or Fall Times	t_r, t_f	–	–	500	ns

DC Electrical Characteristics: (V_{CC} = 5V ±10% unless otherwise specified)

Parameter	Symbol	Test Conditions		T_A = +25°C		T_A = –40° to +85°C	Unit
				Typ	Guaranteed Limits		
Minimum High Level Input Voltage	V_{IH}			–	2.0	2.0	V
Maximum Low Level Input Voltage	V_{IL}			–	0.8	0.8	V
Minimum High Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$\lvert I_{OUT}\rvert = 20\mu A$	V_{CC}	$V_{CC}^{\,-0.1}$	$V_{CC}^{\,-0.1}$	V
			$\lvert I_{OUT}\rvert = 6.0mA$, $V_{CC} = 4.5V$	4.2	3.98	3.84	V
			$\lvert I_{OUT}\rvert = 7.2mA$, $V_{CC} = 5.5V$	5.7	4.98	4.84	V
Maximum Low Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$	$\lvert I_{OUT}\rvert = 20\mu A$	0	0.1	0.1	V
			$\lvert I_{OUT}\rvert = 6.0mA$, $V_{CC} = 4.5V$	0.2	0.26	0.33	V
			$\lvert I_{OUT}\rvert = 7.2mA$, $V_{CC} = 5.5V$	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	$V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL}		–	±0.1	±1.0	µA
Maximum 3–STATE Output Leakage Current	I_{OZ}	$V_{OUT} = V_{CC}$ or GND, $\overline{G} = V_{IH}$, $G = V_{IL}$		–	±0.5	±5.0	µA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$		–	8.0	80	µA
		V_{IN} = 2.4V or 0.5V, Note 4		–	1.0	1.3	mA

Note 4. This is measured per input with all other inputs held at V_{CC} or GND.

AC Electrical Characteristics: (V_{CC} = 5V, $t_r = t_f$ = 6ns, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Maximum Clock Frequency	f_{MAX}		50	30	MHz
Maximum Propagation Delay to Output	t_{PHL}, t_{PLH}	C_L = 45pF	20	32	ns
Maximum Enable Propagation Delay, Control to Output	t_{PZH}, t_{PZL}	C_L = 45pF, R_L = 1kΩ	19	28	ns
Maximum Disable Propagation Delay, Control to Output	t_{PLZ}, t_{PHZ}	C_L = 5pF, R_L = 1kΩ	17	25	ns
Minimum Clock Pulse Width	t_W		–	20	ns
Minimum Setup Time Data to Clock	t_S		–	5	ns
Minimum Hold Time Clock to Data	t_H		–	16	ns

AC Electrical Characteristics: (V_{CC} = 5V ±10%, $t_r = t_f$ = 6ns unless otherwise specified)

Parameter	Symbol	Test Conditions	T_A = +25°C		T_A = –40° to +85°C	Unit
			Typ	Guaranteed Limits		
Maximum Clock Frequency	f_{MAX}		–	30	24	MHz
Maximum Propagation Delay to Output	t_{PHL}, t_{PLH}	C_L = 50pF	22	36	45	ns
		C_L = 150pF	30	46	57	ns
Maximum Enable Propagation Delay Control to Output	t_{PHL}, t_{PLH}	C_L = 50pF	21	30	37	ns
		C_L = 150pF	30	40	50	ns

AC Electrical Characteristics (Cont'd): (V_{CC} = 5V ±10%, $t_r = t_f$ = 6ns unless otherwise specified)

Parameter	Symbol	Test Conditions	T_A = +25°C	T_A = −40° to +85°C		Unit
			Typ	Guaranteed Limits		
Maximum Disable Propagation Delay Control to Output	t_{PHZ}, t_{PLZ}	R_L = 1kΩ, C_L = 50pF	21	30	37	ns
Maximum Output Rise and Fall Time	t_{THL}, t_{TLH}	C_L = 50pF	8	12	15	ns
Minimum Clock Pulse Width	t_W		–	16	20	ns
Minimum Setup Time Data to Clock	t_S		–	20	25	ns
Minimum Hold Time Clock to Data	t_H		–	5	5	ns
Maximum Input Capacitance	C_{IN}		–	10	10	pF
Maximum Output Capacitance	C_{OUT}		–	20	20	pF
Power Dissipation Capacitance (Note 5)	C_{PD}	OC = V_{CC}	5	–	–	pF
		OC = GND	58	–	–	pF

Note 5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table:

Output Control	LE	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH Level
L = LOW Level
X = Don't Care
↑ = Transition from LOW−to−HIGH
Q_0 = Level of output before steady−state input conditions were established.
Z = High Impedance

Pin Connection Diagram