



ELECTRONICS, INC.
 44 FARRAND STREET
 BLOOMFIELD, NJ 07003
 (973) 748-5089
<http://www.nteinc.com>

NTE74HC4040 Integrated Circuit TTL – High Speed CMOS, 12–Stage Binary Counter

Description:

The NTE74HC4040 is a 12–stage ripple–carry binary counter in a 16–Lead DIP type package. All counter stages are master–slave flip–flops. The state of the stage advances one count on the negative clock transition of each input pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

Features:

- Wide Power Supply Range: 2V to 6V
- High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- Fully Static Operation
- Buffered Inputs
- Common Reset
- Negative Edge Clocking
- Fanout (Over Temperature Range):
 - Standard Outputs . . . 10 LS–TTL Loads
 - Bus Driver Outputs . . 15 LS–TTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LS–TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC}	–0.5 to +7.0V
Clamp Diode Current, I_{IK} , I_{OK}	±20mA
DC Output Source or Sink Current (Per Output), I_{OUT}	±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC}	±50mA
Maximum Junction, T_J	+150°C
Storage Temperature Range, T_{stg}	–65°C to +150°C
Typical Thermal Resistance, Junction–to–Ambient, R_{thJA}	67°C/W
Lead Temperature (During Soldering, 10sec), T_L	+300°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
 Note 2. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C
Input Rise or Fall Times $V_{CC} = 2.0V$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$	t_r, t_f	–	–	1000	ns
		–	–	500	ns
		–	–	400	ns

DC Electrical Characteristics:

Parameter	Symbol	Test Conditions	V_{CC}	$T_A = +25^\circ C$		$T_A = -40^\circ \text{ to } +85^\circ C$		Unit
				Typ	Guaranteed Limits			
Minimum High Level Input Voltage	V_{IH}		2.0	–	1.5	1.5	V	
			4.5	–	3.15	3.15	V	
			6.0	–	4.2	4.2	V	
Maximum Low Level Input Voltage	V_{IL}		2.0	–	0.5	0.5	V	
			4.5	–	1.35	1.35	V	
			6.0	–	1.8	1.8	V	
Minimum High Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OUT} = -20\mu A$	–	V_{CC}	$V_{CC}^{-0.1}$	$V_{CC}^{-0.1}$	V
			$I_{OUT} = -4mA$	4.5	–	3.98	3.84	V
			$I_{OUT} = -5.2mA$	6.0	–	5.48	5.34	V
Minimum Low Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$	$I_{OUT} = 20\mu A$	–	0	0.1	0.1	V
			$I_{OUT} = 4mA$	4.5	–	0.26	0.33	V
			$I_{OUT} = 5.2mA$	6.0	–	0.26	0.33	V
Maximum Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	–	± 0.1	± 1.0	μA	
Maximum Quiescent Device Current	I_{CC}	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0mA$	6.0	–	8.0	80	μA	

Prerequisite for Switching Specifications:

Parameter	Symbol	Test Conditions	V_{CC}	$T_A = +25^\circ C$		$T_A = -40^\circ \text{ to } +85^\circ C$		Unit
				Typ	Guaranteed Limits			
Maximum Pulse Frequency	f_{MAX}		2.0	–	6	5	MHz	
			4.5	–	30	25	MHz	
			6.0	–	35	29	MHz	
Input Pulse Width	t_W		2.0	–	80	100	ns	
			4.5	–	16	20	ns	
			6.0	–	14	17	ns	
Reset Removal Time	t_{REM}		2.0	–	50	65	ns	
			4.5	–	10	13	ns	
			6.0	–	9	11	ns	
Reset Pulse Width	t_W		2.0	–	80	100	ns	
			4.5	–	16	20	ns	
			6.0	–	14	17	ns	

Switching Specifications: ($t_r = t_f = 6\text{ns}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	V _{CC}	T _A = +25°C		T _A = -40° to +85°C		Unit
				Typ	Guaranteed Limits			
Propagation Delay Time (CP to Q1' Output)	t _{PLH} , t _{PHL}	C _L = 50pF	2.0	-	140	175	ns	
			4.5	-	28	35	ns	
		C _L = 15pF	5.0	11	-	-	ns	
		C _L = 50pF	6.0	-	24	30	ns	
Propagation Delay Time (Q _n to Q _{n+1})	t _{PLH} , t _{PHL}	C _L = 50pF	2.0	-	75	95	ns	
			4.5	-	15	19	ns	
		C _L = 15pF	5.0	4	-	-	ns	
		C _L = 50pF	6.0	-	13	16	ns	
Propagation Delay Time (MR to Q _n)	t _{PLH} , t _{PHL}	C _L = 50pF	2.0	-	170	215	ns	
			4.5	-	34	43	ns	
		C _L = 15pF	5.0	14	-	-	ns	
		C _L = 50pF	6.0	-	29	37	ns	
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	2.0	-	75	95	ns	
			4.5	-	15	19	ns	
			6.0	-	13	16	ns	
Maximum Input Capacitance	C _{IN}	C _L = 50pF	-	-	10	10	pF	
Power Dissipation Capacitance	C _{PD}	C _L = 15pF, Note 3	5.0	40	-	-	pF	

Note 3. C_{PD} is used to determine the dynamic power consumption, per package.
 $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_i / M)$ where $M = 2^1, 2^2, 2^3, \dots, 2^{12}$, f_i = Input Frequency,
 C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Truth Table:

CP Count	MR	Output State
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs are Low

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

↑ = Transition from LOW to HIGH Level

↓ = Transition from HIGH to LOW Level

Pin Connection Diagram

