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NTE74HC390 Integrated Circuit TTL – High Speed CMOS, Dual Decade Ripple Counter

Description:

The NTE74HC390 is a dual 4-bit decade ripple counter in a 16-Lead DIP type package and is pin compatible with low-power Schottky TTL (LS-TTL). This device is divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clock inputs (nCP0 and nCP1) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100. Each section is triggered by the High-to-Low transition of the input pulses (nCP0 and nCP1).

For BCD decade operation, the nQ0 output is connected to the nCP1 input of the divide-by-5 section. For bi-quinary decade operation, the nQ3 output is connected to the nCP0 input and nQ0 becomes the decade output.

The master reset inputs (1MR and 2MR) are active-High asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A High level on the nMR input overrides the clock and sets the four outputs Low.

Features:

- Wide Power Supply Range: 2V to 6V
- High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- Two BCD Decades or Bi-Quinary Counters
- One package can be Configured to Divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two Master Reset Inputs to Clear Each Decade Counter Individually
- Fanout (Over Temperature Range):
 - Standard Outputs . . . 10 LS-TTL Loads
 - Bus Driver Outputs . . 15 LS-TTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LS-TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC}	-0.5 to +7.0V
Clamp Diode Current, I_{IK} , I_{OK}	±20mA
DC Output Source or Sink Current (Per Output), I_{OUT}	±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC}	±50mA
Maximum Junction, T_J	+150°C
Storage Temperature Range, T_{stg}	-65°C to +150°C
Typical Thermal Resistance, Junction-to-Ambient, R_{thJA}	67°C/W
Lead Temperature (During Soldering, 10sec), T_L	+300°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit	
Supply Voltage	V_{CC}	2.0	–	6.0	V	
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V	
Operating Temperature Range	T_A	–55	–	+85	°C	
Input Rise or Fall Times $V_{CC} = 2.0V$	t_r, t_f	–	–	1000	ns	
		$V_{CC} = 4.5V$	–	–	500	ns
		$V_{CC} = 6.0V$	–	–	400	ns

DC Electrical Characteristics:

Parameter	Symbol	Test Conditions	V_{CC}	$T_A = +25^\circ C$		$T_A = -40^\circ \text{ to } +85^\circ C$		Unit
				Typ	Guaranteed Limits			
Minimum High Level Input Voltage	V_{IH}		2.0	–	1.5	1.5	V	
			4.5	–	3.15	3.15	V	
			6.0	–	4.2	4.2	V	
Maximum Low Level Input Voltage	V_{IL}		2.0	–	0.5	0.5	V	
			4.5	–	1.35	1.35	V	
			6.0	–	1.8	1.8	V	
Minimum High Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OUT} = -20mA$	–	V_{CC}	$V_{CC}^{-0.1}$	$V_{CC}^{-0.1}$	V
			$I_{OUT} = -4mA$	4.5	–	3.98	3.84	V
			$I_{OUT} = -5.2A$	6.0	–	5.48	5.34	V
Minimum Low Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$	$I_{OUT} = 20mA$	–	0	0.1	0.1	V
			$I_{OUT} = 4mA$	4.5	–	0.26	0.33	V
			$I_{OUT} = 5.2A$	6.0	–	0.26	0.33	V
Maximum Input Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	–	± 0.1	± 1.0	μA	
Maximum Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0mA$	6.0	–	8.0	80	μA	

Prerequisite for Switching Specifications:

Parameter	Symbol	Test Conditions	V_{CC}	$T_A = +25^\circ C$		$T_A = -40^\circ \text{ to } +85^\circ C$		Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency	f_{MAX}		2.0	–	6	5	MHz	
			4.5	–	30	24	MHz	
			6.0	–	35	28	MHz	
Clock Pulse Width ($\overline{nCP0}, \overline{nCP1}$)	t_W		2.0	–	80	100	ns	
			4.5	–	16	20	ns	
			6.0	–	14	17	ns	
Minimum Reset Removal Time	t_{REM}		2.0	–	70	90	ns	
			4.5	–	14	18	ns	
			6.0	–	12	15	ns	
Minimum Reset Pulse Width	t_W		2.0	–	50	65	ns	
			4.5	–	10	13	ns	
			6.0	–	9	11	ns	

Switching Specifications: ($t_r = t_f = 6\text{ns}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	V _{CC}	T _A = +25°C		T _A = -40° to +85°C		Unit
				Typ	Guaranteed Limits			
Propagation Delay Time (nCP0 to nQ0)	t _{PLH} , t _{PHL}	C _L = 50pF	2.0	-	175	220	ns	
			4.5	-	35	44	ns	
		C _L = 15pF	5.0	14	-	-	ns	
		C _L = 50pF	6.0	-	30	37	ns	
Propagation Delay Time (nCP1 to nQ1)	t _{PLH} , t _{PHL}	C _L = 50pF	2.0	-	185	230	ns	
			4.5	-	37	46	ns	
			6.0	-	31	39	ns	
Propagation Delay Time (nCP1 to nQ2)	t _{PLH} , t _{PHL}	C _L = 50pF	2.0	-	245	305	ns	
			4.5	-	49	61	ns	
			6.0	-	42	52	ns	
Propagation Delay Time (nCP1 to nQ3)	t _{PLH} , t _{PHL}	C _L = 50pF	2.0	-	180	225	ns	
			4.5	-	36	45	ns	
		C _L = 15pF	5.0	15	-	-	ns	
		C _L = 50pF	6.0	-	31	38	ns	
Propagation Delay Time (nCP0 to nQ3) (nQ0 connected to nCP1)	t _{PLH} , t _{PHL}	C _L = 50pF	2.0	-	365	455	ns	
			4.5	-	73	91	ns	
			6.0	-	62	77	ns	
Propagation Delay Time (MR to nQn)	t _{PLH} , t _{PHL}	C _L = 50pF	2.0	-	190	240	ns	
			4.5	-	38	48	ns	
		C _L = 15pF	5.0	16	-	-	ns	
		C _L = 50pF	6.0	-	32	41	ns	
Output Transition Time, Q0, Q7	t _{TLH} , t _{THL}	C _L = 50pF	2.0	-	75	95	ns	
			4.5	-	15	19	ns	
			6.0	-	13	16	ns	
Maximum Input Capacitance	C _{IN}	C _L = 50pF	-	-	10	10	pF	
Power Dissipation Capacitance	C _{PD}	C _L = 15pF, Note 3	5.0	28	-	1-	pF	

Note 3. C_{PD} is used to determine the dynamic power consumption, per multiplexer.
 $P_D = P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance,
 V_{CC} = Supply Voltage.

Truth Table:

Inputs		Action
CP	MR	
↑	L	No Change
↓	L	Count
X	X	All Qs Low

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

↑ = Transition from LOW-to-HIGH level

↓ = Transition from HIGH-to-LOW level

BCD Count Sequence for 1/2 The Device:

Count	Outputs			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Output nQ0 connected to nCP1 with counter input on nCP0.

B-Quinary Count Sequence for 1/2 The Device:

Count	Outputs			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	H	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

Output nQ3 connected to nCP0 with counter input on nCP1.

Pin Connection Diagram



