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NTE74HC377 Integrated Circuit TTL – High Speed CMOS, Octal D–Type Flip–Flop with Common Enable

Description:

The NTE74HC377 is a high speed octal D–type flip–flop in a 20–Lead DIP type package with a buffered clock (CP) common to all eight flip–flops. All the flip–flops are loaded simultaneously on the positive edge of the clock (CP) when the Data Enable (\bar{E}) is LOW.

Features:

- Wide Power Supply Range: 2V to 6V
- High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- Buffered Common Clock
- Buffered Inputs
- Typical Propagation Delay: 14ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = +25^\circ C$
- Fanout (Over Temperature Range):
 - Standard Outputs . . . 10 LS–TTL Loads
 - Bus Driver Outputs . . 15 LS–TTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LS–TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC}	–0.5 to +7.0V
Clamp Diode Current, I_{IK} , I_{OK}	±20mA
DC Output Source or Sink Current (Per Output), I_{OUT}	±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC}	±50mA
Maximum Junction, T_J	+150°C
Storage Temperature Range, T_{stg}	–65°C to +150°C
Typical Thermal Resistance, Junction–to–Ambient, R_{thJA}	69°C/W
Lead Temperature (During Soldering, 10sec), T_L	+300°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
 Note 2. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	-	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	-	V_{CC}	V
Operating Temperature Range	T_A	-40	-	+85	°C
Input Rise or Fall Times $V_{CC} = 2.0V$	t_r, t_f	-	-	1000	ns
$V_{CC} = 4.5V$		-	-	500	ns
$V_{CC} = 6.0V$		-	-	400	ns

DC Electrical Characteristics:

Parameter	Symbol	Test Conditions	V_{CC}	$T_A = +25^\circ C$		$T_A = -40^\circ \text{ to } +85^\circ C$		Unit
				Typ	Guaranteed Limits	Typ	Guaranteed Limits	
Minimum HIGH Level Input Voltage	V_{IH}		2.0	-	1.5	1.5	V	
			4.5	-	3.15	3.15	V	
			6.0	-	4.2	4.2	V	
Maximum LOW Level Input Voltage	V_{IL}		2.0	-	0.5	0.5	V	
			4.5	-	1.35	1.35	V	
			6.0	-	1.8	1.8	V	
Minimum HIGH Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OUT} = -20\mu A$	-	V_{CC}	$V_{CC}^{-0.1}$	$V_{CC}^{-0.1}$	V
			$I_{OUT} = -6mA$	4.5	-	3.98	3.84	V
			$I_{OUT} = -7.8mA$	6.0	-	5.48	5.34	V
Minimum LOW Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OUT} = 20\mu A$	-	-	0.1	0.1	V
			$I_{OUT} = 6mA$	4.5	0.2	0.26	0.33	V
			$I_{OUT} = 7.8mA$	6.0	0.2	0.26	0.33	V
Maximum Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	-	± 0.1	± 1.0	μA	
Maximum Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	6.0	-	8.0	80	μA	

Prerequisite for Switching Specifications:

Parameter	Symbol	Test Conditions	V_{CC}	$T_A = +25^\circ C$		$T_A = -40^\circ \text{ to } +85^\circ C$		Unit
				Typ	Guaranteed Limits	Typ	Guaranteed Limits	
Maximum Clock Frequency	f_{MAX}		2.0	-	6	5	MHz	
			4.5	-	30	25	MHz	
			6.0	-	35	29	MHz	
Clock Pulse Width	t_w		2.0	-	80	100	ns	
			4.5	-	16	20	ns	
			6.0	-	14	17	ns	
Setup Time (\bar{E} , Data to CP)	t_{SU}		2.0	-	60	75	ns	
			4.5	-	12	15	ns	
			6.0	-	10	13	ns	
Hold Time (Data to CP)	t_H		2.0	-	3	3	ns	
			4.5	-	3	3	ns	
			6.0	-	3	3	ns	
Hold Time (\bar{E} to CP)	t_H		2.0	-	5	5	ns	
			4.5	-	5	5	ns	
			6.0	-	5	5	ns	

Switching Specifications: ($t_r = t_f = 6\text{ns}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	V _{CC}	T _A = +25°C		T _A = -40° to +85°C		Unit
				Typ	Guaranteed Limits			
Propagation Delay Time (CP to Q)	t _{PLH} , t _{PHL}	C _L = 50pF	2.0	-	175	220	ns	
			4.5	-	35	44	ns	
		C _L = 15pF	5.0	14	-	-	ns	
		C _L = 50pF	6.0	-	30	37	ns	
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	2.0	-	75	95	ns	
			4.5	-	15	19	ns	
			6.0	-	13	16	ns	
Maximum Input Capacitance	C _{IN}		-	-	10	10	pF	
Maximum Clock Frequency	f _{MAX}	C _L = 15pF	5.0	60	-	-	MHz	
Power Dissipation Capacitance	C _{PD}	C _L = 15pF, Note 3	5.0	31	-	-	pF	

Note 3. C_{PD} is used to determine the dynamic power consumption, per flip-flop.
 $P_D = C_{PD} V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Truth Table:

Operation Mode	Inputs			Outputs
	CP	\bar{E}	D _n	Q _n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level (Steady State)
h = High Voltage Level One Set-Up Time Prior to the Low to High Clock Transition
L = LOW Voltage Level (Steady State)
l = Low Voltage Level One Set-Up Time Prior to the Low to High Clock Transition
X = Don't Care
↑ = Transition from LOW to HIGH Level

Pin Connection Diagram

