NTE
ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748−5089
http://www.nteinc.com

NTE74HC175
Integrated Circuit
TTL − High Speed CMOS,
Quad D−Type Flip−Flop with Common Direct Clear and Complementary Outputs

Description:

The NTE74HC175 is a high speed D−type flip−flop with complementary outputs in a 16−Lead DIP type package that utilizes advanced silicon−gate CMOS technology to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS−TTL loads.

Information at the D inputs is transferred to the Q and $\overline{Q}$ outputs on the positive going edge of the clock pulse. Both true and complement outputs from each flip−flop are externally available. All four flip−flops are controlled by a common clock and a common CLEAR. Clearing is accomplished by a negative pulse at the CLEAR input. All four Q outputs are cleared to a logical “0” and all four $\overline{Q}$ outputs to a logical “1”.

The 74HC logic family is functionally as well as pin−out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and GND.

Features:

- Typical Propagation Delay: 15ns
- Wide Power Supply Range: 2V to 6V
- Low Input Current: 1μA (max)
- Low Quiescent Current: 80μA (max)
- High Output Drive Current: 4mA (min)

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC}	−0.5 to +7.0V
DC Input Voltage, V_{IN}	−1.5 to V_{CC} +1.5V
DC Output Voltage, V_{OUT}	−0.5 to V_{CC} + 0.5V
Clamp Diode Current, I_{IK}, I_{OK}	±20mA
DC Output Current (Per Pin), I_{OUT}	±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC}	±50mA
Power Dissipation (Note 3), P_D	600mW
Storage Temperature Range, T_{stg}	−65°C to +150°C
Lead Temperature (During Soldering, 10sec), T_L	+260°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.
Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C
Input Rise or Fall Times V_{CC} = 2.0V	t_r, t_f	–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics: (Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions		V_{CC}	T_A = +25°C		T_A = –40° to +85°C	Unit
					Typ	Guaranteed Limits		
Minimum HIGH Level Input Voltage	V_{IH}			2.0	–	1.5	1.5	V
				4.5	–	3.15	3.15	V
				6.0	–	4.2	4.2	V
Maximum LOW Level Input Voltage	V_{IL}			2.0	–	0.5	0.5	V
				4.5	–	1.35	1.35	V
				6.0	–	1.8	1.8	V
Minimum HIGH Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$\|I_{OUT}\| \le 20\mu A$	–	V_{CC}	$V_{CC}^{-0.1}$	$V_{CC}^{-0.1}$	V
			$\|I_{OUT}\| \le 4.0mA$	4.5	4.2	3.98	3.84	V
			$\|I_{OUT}\| \le 5.2mA$	6.0	5.7	5.48	5.34	V
Minimum LOW Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$	$\|I_{OUT}\| \le 20\mu A$	–	0	0.1	0.1	V
			$\|I_{OUT}\| \le 4.0mA$	4.5	0.2	0.26	0.33	V
			$\|I_{OUT}\| \le 5.2mA$	6.0	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	$V_{IN} = V_{CC}$ or GND		6.0	–	±0.1	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$		6.0	–	8.0	80	µA

Note 4. For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively (The V_{IH} value at 5.5V is 3.85V). The worst case leakage current (I_{IN}, I_{CC} and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics: V_{CC} = 5V, $t_r = t_f$ = 6ns, C_L = 15pF, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Maximum Operating Frequency	f_{MAX}		60	30	ns
Maximum Propagation Delay (Clock to Q or $\overline{Q}$)	t_{PHL}, t_{PLH}		15	25	ns
Maximum Propagation Delay (Reset to Q or $\overline{Q}$)	t_{PHL}, t_{PLH}		13	21	ns
Minimum Removal Time (Clear to Clock)	t_{REM}		–	20	ns
Minimum Set Up Time (Data to Clock)	t_S		–	20	ns
Minimum Hold Time (Clock to Data)	t_H		–	0	ns
Minimum Pulse Width (Clock or Clear)	t_W		10	16	ns

AC Electrical Characteristics: (t_r = t_f = 6ns, C_L = 50pF unless otherwise specified)

				T_A = +25°C		T_A = –40° to +85°C	
Parameter	**Symbol**	**Test Conditions**	**V_{CC}**	**Typ**	**Guaranteed Limits**		**Unit**
Maximum Operating Frequency	f_{MAX}		2.0	12	6	5	MHz
			4.5	60	30	24	MHz
			6.0	70	35	28	MHz
Maximum Propagation Delay (Clock to Q or $\overline{Q}$)	t_{PHL}, t_{PLH}		2.0	80	150	190	ns
			4.5	15	30	38	ns
			6.0	13	26	32	ns
Maximum Propagation Delay (Reset to Q or $\overline{Q}$)	t_{PHL}, t_{PLH}		2.0	64	125	158	ns
			4.5	14	25	32	ns
			6.0	12	21	27	ns
Minimum Removal Time (Clear to Clock)	t_{REM}		2.0	–	100	125	ns
			4.5	–	20	25	ns
			6.0	–	17	21	ns
Minimum Setup Time (Data to Clock)	t_S		2.0	–	100	125	ns
			4.5	–	20	25	ns
			6.0	–	17	21	ns
Minimum Hold Time (Clock to Data)	t_H		2.0	–	0	0	ns
			4.5	–	0	0	ns
			6.0	–	0	0	ns
Minimum Pulse Width (Clock or Clear)	t_W		2.0	30	80	100	ns
			4.5	9	16	20	ns
			6.0	8	14	17	ns
Maximum Output Rise and Fall Time	t_{THL}, t_{TLH}		2.0	30	75	95	ns
			4.5	9	15	19	ns
			6.0	8	13	16	ns
Maximum Input Rise and Fall Time	t_r, t_f		2.0	–	1000	1000	ns
			4.5	–	500	500	ns
			6.0	–	400	400	ns
Power Dissipation Capacitance	C_{PD}	Per Package, Note 5	–	150	–	–	pF
Maximum Input Capacitance	C_{IN}		–	5	10	10	pF

Note 5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table:

Inputs			**Outputs**	
Clear	**Clock**	**D**	**Q**	**$\overline{Q}$**
L	X	X	L	L
H	↑	H	H	H
H	↑	L	L	L
H	L	X	Q_O	$\overline{Q}_O$

H = HIGH Level
L = LOW Level
X = Irrelevant (any input, including transitions)
↑ = Transition from LOW–to–HIGH level

Q_{AO} = the level of Q before the indicated steady state input conditions were established.

Pin Connection Diagram