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NTE74HC164
Integrated Circuit
TTL – High Speed CMOS,
8–Bit Serial–In/Parallel–Out Shift Register

Description:

The NTE74HC164 is an 8–bit serial–in/parallel–out shift register in a 14–Lead DIP type package that utilize advanced silicon–gate CMOS technology. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8–bit shift register has gated serial inputs and CLEAR. Each register bit is a D–type master/slave flip–flop. Input A & B permit complete control over the incoming data. A LOW at either or both inputs inhibits entry of new data and resets the first flip–flop to the low level at the next clock pulse. A high level on one input enables the other input which then determines the state of the first flip–flop. Data at the serial inputs may be changed while the clock is HIGH or LOW, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8–bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

The 74HC logic family is functionally as well as pin–out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and GND.

Features:

- Typical Operating Frequency: 50MHz
- Typical Propagation Delay: Clock to Q: 19ns
- Low Quiescent Current: 80μA (max)
- Low Input Current: 1μA (max)
- Wide Power Supply Range: 2V to 6V

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
DC Input Voltage, V_{IN} . . . . . –1.5 to V_{CC} +1.5V
DC Output Voltage, V_{OUT} . . . . . –0.5 to V_{CC} + 0.5V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Power Dissipation (Note 3), P_D 600mW
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.
Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–55	–	+85	°C
Input Rise or Fall Times	t_r, t_f				
V_{CC} = 2.0V		–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics: (Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions		V_{CC}	T_A = +25°C	T_A = –40° to +85°C		Unit
					Typ	Guaranteed Limits		
Minimum High Level Input Voltage	V_{IH}			2.0	–	1.5	1.5	V
				4.5	–	3.15	3.15	V
				6.0	–	4.2	4.2	V
Maximum Low Level Input Voltage	V_{IL}			2.0	–	0.5	0.5	V
				4.5	–	1.35	1.35	V
				6.0	–	1.8	1.8	V
Minimum High Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	$\|I_{OUT}\| \le 20\mu A$	–	V_{CC}	V_{CC} –0.1	V_{CC} –0.1	V
			$\|I_{OUT}\| \le 4.0mA$	4.5	4.2	3.98	3.84	V
			$\|I_{OUT}\| \le 5.2mA$	6.0	5.7	5.48	5.34	V
Minimum Low Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	$\|I_{OUT}\| \le 20\mu A$	–	0	0.1	0.1	V
			$\|I_{OUT}\| \le 4.0mA$	4.5	0.2	0.26	0.33	V
			$\|I_{OUT}\| \le 5.2mA$	6.0	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	±0.1	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		6.0	–	8.0	80	μA

Note 4. For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively (The V_{IH} value at 5.5V is 3.85V). The worst case leakage current (I_{IN}, I_{CC} and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics: (V_{CC} = 5V, t_r = t_f = 6ns, C_L = 15pF, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Maximum Operating Frequency	f_{MAX}		–	30	ns
Maximum Propagation Delay (Clock to Output)	t_{PHL}, t_{PLH}		19	30	ns
Maximum Propagation Delay (Clear to Output)	t_{PHL}		23	35	ns
Maximum Removal Time (Clear to Clock)	t_{REM}		–2	0	ns
Minimum Set Up Time (Data to Clock)	t_S		12	20	ns
Minimum Hold Time (Clock to Data)	t_H		1	5	ns
Minimum Pulse Width (Clear or Clock)	t_W		10	16	ns

AC Electrical Characteristics: ($t_r = t_f$ = 6ns, C_L = 50pF unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
				Typ	Guaranteed Limits		
Maximum Operating Frequency	f_{MAX}		2.0	–	5	4	MHz
			4.5	–	27	21	MHz
			6.0	–	32	25	MHz
Maximum Propagation Delay (Clock to Output)	t_{PHL}, t_{PLH}		2.0	115	175	218	ns
			4.5	13	35	44	ns
			6.0	20	30	38	ns
Maximum Propagation Delay (Clear to Output)	t_{PHL}		2.0	140	205	256	ns
			4.5	28	41	51	ns
			6.0	24	35	44	ns
Minimum Removal Time (Clear to Clock)	t_{REM}		2.0	−7	0	0	ns
			4.5	−3	0	0	ns
			6.0	−2	0	0	ns
Minimum Setup Time (Data to Clock)	t_S		2.0	25	100	125	ns
			4.5	14	20	25	ns
			6.0	12	17	21	ns
Minimum Hold Time (Clock to Data)	t_H		2.0	−2	5	5	ns
			4.5	0	5	5	ns
			6.0	1	5	5	ns
Minimum Pulse Width (Clear or Clock)	t_W		2.0	22	80	100	ns
			4.5	11	16	20	ns
			6.0	10	14	18	ns
Maximum Output Rise and Fall Time	t_{THL}, t_{TLH}		2.0	–	75	95	ns
			4.5	–	15	19	ns
			6.0	–	13	16	ns
Maximum Input Rise and Fall Time	t_r, t_f		2.0	–	1000	1000	ns
			4.5	–	500	500	ns
			6.0	–	400	400	ns
Power Dissipation Capacitance	C_{PD}	Per Package, Note 5	–	150	–	–	pF
Maximum Input Capacitance	C_{IN}		–	5	10	10	pF

Note 5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table:

Inputs				Outputs	
Clear	**Clock**	**A**	**B**	**Q_A**	**Q_B . . . Q_H**
L	X	X	X	L	L . . . L
H	L	X	X	Q_{AO}	Q_{BO} . . . Q_{HO}
H	↑	H	H	H	Q_{An} . . . Q_{Gn}
H	↑	L	X	L	Q_A . . . Q_{Gn}
H	↑	X	L	L	Q_{An} . . . Q_{Gn}

H = HIGH Level (Steady State)

L = LOW Level (Steady State)

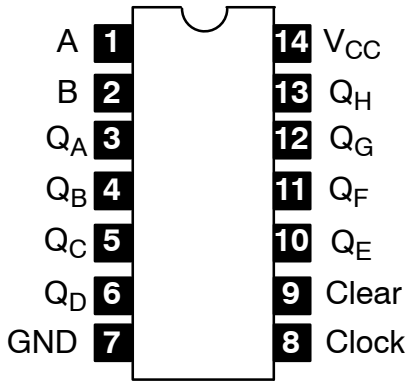
X = Irrelevant (any input, including transitions)

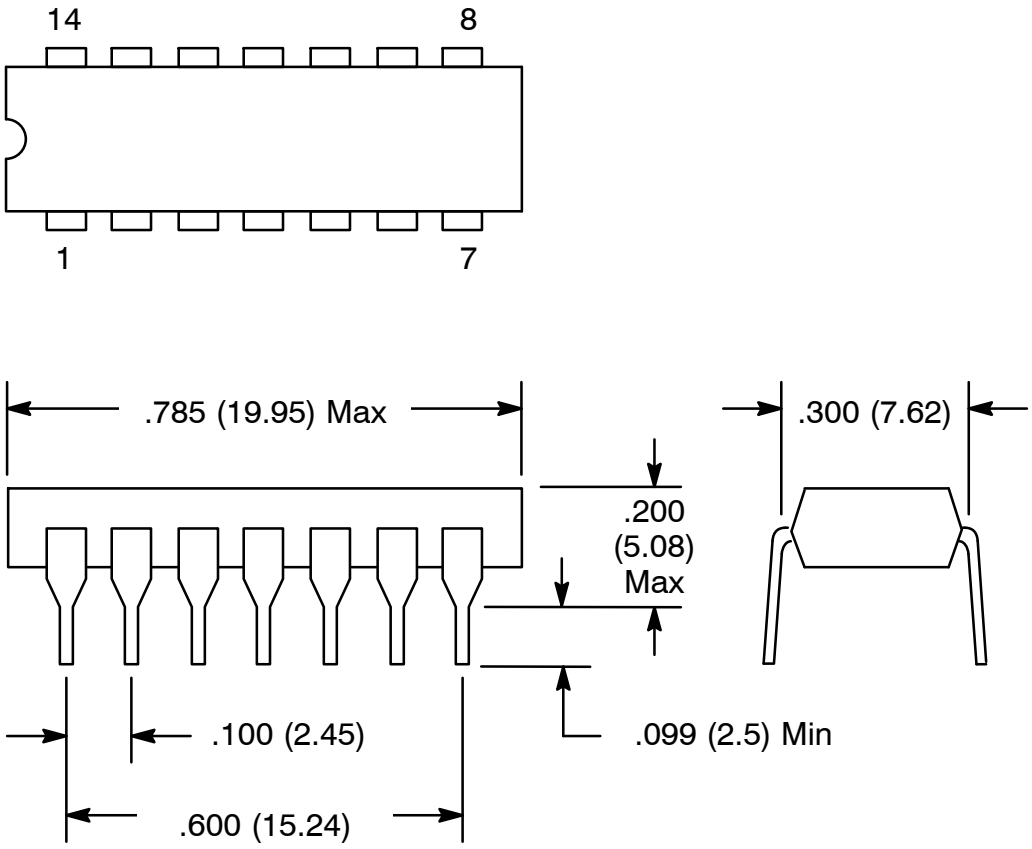
↑ = Transition from LOW−to−HIGH level

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one−bit shift.

Pin Connection Diagram




14
8
1
7
.785 (19.95) Max
.300 (7.62)
.200
(5.08)
Max
.100 (2.45)
.099 (2.5) Min
.600 (15.24)