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NTE74HCT139 Integrated Circuit TTL – High Speed CMOS, Dual 2-to-4 Line Decoder/Demultiplexer

Description:

The NTE74HCT138 is a dual 2-to-4 line decoder in a 16-Lead plastic DIP type package that utilizes advanced silicon-gate CMOS technology, and is well suited to memory address decoding or data routing applications. It possesses the high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky logic.

The NTE74HC139 contains two independent one-of-four decoders each with a single active low enable input (G1 or G2). Data on the select inputs (A1 and B1 or A2 and B2) cause one of the four normally high outputs to go LOW.

The decoder's outputs can drive 10 low power Schottky TTL equivalent loads and are functionally, as well as pin equivalent, to the NTE74LS139. All inputs are protected from damage due to static discharge by diodes to V_{CC} and GND.

Features:

- Typical Propagation Delays —
 - Select to Output (4 Delays): 18ns
 - Select to Output (5 Delays): 28ns
 - Enable to Output: 20ns
- Low Power: 40μW Quiescent Supply Power
- Fanout of 10 LS-TTL Loads
- Wide Power Supply Range: 2V to 6V
- Input Current: 1μA (max), 10pA (typ)

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V _{CC}	-0.5 to +7.0V
DC Input Voltage, V _{IN}	-1.5 to V _{CC} +1.5V
DC Output Voltage, V _{OUT}	-0.5 to V _{CC} + 0.5V
Clamp Diode Current, I _{IK} , I _{OK}	±20mA
DC Output Current (Per Pin), I _{OUT}	±25mA
DC V _{CC} or GND Current (Per Pin), I _{CC}	±50mA
Power Dissipation (Note 3), P _D	600mW
Storage Temperature Range, T _{stg}	-65°C to +150°C
Lead Temperature (During Soldering, 10sec), T _L	+260°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
 Note 2. Unless otherwise specified, all voltages are referenced to GND.
 Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	-	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	-	V_{CC}	V
Operating Temperature Range	T_A	-40	-	+85	°C
Input Rise or Fall Times $V_{CC} = 2.0V$	t_r, t_f	-	-	1000	ns
$V_{CC} = 4.5V$		-	-	500	ns
$V_{CC} = 6.0V$		-	-	400	ns

DC Electrical Characteristics: ($V_{CC} = 5V \pm 10\%$, Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C		-40° to +85°C		-40° to +125°C		Unit
				Typ	Guaranteed Limits					
Minimum HIGH Level Input Voltage	V_{IH}		2.0	-	1.5	1.5	1.5	V		
			4.5	-	3.15	3.15	3.15	V		
			6.0	-	4.2	4.2	4.2	V		
Maximum LOW Level Input Voltage	V_{IL}		2.0	-	0.5	0.5	0.5	V		
			4.5	-	1.35	1.35	1.35	V		
			6.0	-	1.8	1.8	1.8	V		
Minimum HIGH Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL} , $ I_{OUT} \leq 20\mu A$	2.0	2.0	1.9	1.9	1.9	V		
			4.5	4.5	4.4	4.4	4.4	V		
			6.0	6.0	5.9	5.9	5.9	V		
		$V_{IN} = V_{IH}$ or V_{IL}	$ I_{OUT} \leq 4.0mA$	4.5	4.2	3.98	3.84	3.70	V	
			$ I_{OUT} \leq 5.2mA$	6.0	5.7	5.48	5.34	5.20	V	
Maximum LOW Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL} , $ I_{OUT} \leq 20\mu A$	2.0	0	0.1	0.1	0.1	V		
			4.5	0	0.1	0.1	0.1	V		
			6.0	0	0.1	0.1	0.1	V		
		$V_{IN} = V_{IH}$ or V_{IL}	$ I_{OUT} \leq 4.0mA$	4.5	0.2	0.26	0.33	0.40	V	
			$ I_{OUT} \leq 5.2mA$	6.0	0.2	0.26	0.33	0.40	V	
Maximum Input Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	-	± 0.1	± 1.0	± 1.0	μA		
Maximum Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	6.0	-	8.0	80	160	μA		

Note 4. For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} and V_{OL}) occur at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively (The V_{IH} value at 5.5V is 3.85V). The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics: ($V_{CC} = 5V$, $t_r = t_f = 6ns$, $C_L = 15pF$, $T_A = +25^\circ C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Maximum Propagation Delay, Binary Select to Any Output 4 Levels of Delay	t_{PHL}, t_{PLH}		18	30	ns
Maximum Propagation Delay, Binary Select to Any Output 5 Levels of Delay	t_{PHL}, t_{PLH}		28	38	ns
Maximum Propagation Delay, Enable to Any Output	t_{PHL}, t_{PLH}		19	30	ns

AC Electrical Characteristics: ($V_{CC} = 5V \pm 10\%$, $t_r = t_f = 6ns$, $C_L = 50pF$ unless otherwise specified)

Parameter	Symbol	Test Conditions	V _{CC} (V)	+25°C	-40° to +85°C	-40° to +125°C	Unit	
				Typ	Guaranteed Limits			
Maximum Propagation Delay, Binary Select to Any Output 4 Levels of Delay	t _{PHL} , t _{PLH}	Note 5	2.0	110	175	219	254	V
			4.5	22	35	44	51	V
			6.0	18	30	38	44	V
Maximum Propagation Delay, Binary Select to Any Output 5 Levels of Delay	t _{PHL} , t _{PLH}	Note 6	2.0	165	275	320	254	V
			4.5	33	44	55	64	V
			6.0	28	38	47	54	V
Maximum Propagation Delay, Enable to Any Output	t _{PHL} , t _{PLH}		2.0	115	175	219	254	V
			4.5	23	35	44	51	V
			6.0	19	30	38	44	V
Maximum Output Rise and Fall Time	t _{THL} , t _{TLH}		2.0	30	75	95	110	V
			4.5	8	15	19	22	V
			6.0	7	13	16	19	V
Power Dissipation Capacitance	C _{PD}	Note 7	-	75	-	-	-	pF
Maximum Input Capacitance	C _{IN}		-	3	10	10	10	pF

Note 5. 4 levels of delay are A to Y1, Y3 and B to Y2, Y3.

Note 6. 5 levels of delay are A to Y0, Y2 and B to Y0, Y1.

Note 7. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table:

Inputs			Outputs			
Enable	Select		Y0	Y1	Y2	Y3
G	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Level

L = LOW Level

X = Don't Care

Pin Connection Diagram

