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NTE74HCT132
Integrated Circuit
TTL – High Speed CMOS,
Quad 2–Input NAND Schmitt Trigger

Description:

The NTE74HCT138 is a quad 2–input NAND Schmitt Trigger in a 14–Lead plastic DIP type package that utilizes advanced silicon–gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS–TTL loads.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and GND..

Features:

- Propagation Delay: 12ns (typ)
- Wide Power Supply Range: 2V to 6V
- Low Quiescent Current: 20μA (max)
- Low Input Current: 1μA (max)
- Fanout of 10 LS–TTL Loads
- Hysteresis Voltage: 0.9V (typ) at V_{CC} = 4.5V

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
DC Input Voltage, V_{IN} . . . . . –1.5 to V_{CC} +1.5V
DC Output Voltage, V_{OUT} . . . . . –0.5 to V_{CC} + 0.5V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Power Dissipation (Note 3), P_D 600mW
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.
Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+125	°C

DC Electrical Characteristics: (V_{CC} = 5V ±10%, Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions		V_{CC} (V)	+25°C	–40° to +85°C	–40° to +125°C		Unit
					Typ	Guaranteed Limits			
Positive Going ThresholdVoltage	V_{T+}		Min	2.0	–	1.0	1.0	1.0	V
				4.5	–	2.0	2.0	2.0	V
				6.0	–	3.0	3.0	3.0	V
			Max	2.0	–	1.5	1.5	1.5	V
				4.5	–	3.15	3.15	3.15	V
				6.0	–	4.2	4.2	4.2	V
Negative Going ThresholdVoltage	V_{T-}		Min	2.0	–	0.3	0.3	0.3	V
				4.5	–	0.9	0.9	0.9	V
				6.0	–	1.2	1.2	1.2	V
			Max	2.0	–	1.0	1.0	1.0	V
				4.5	–	2.2	2.2	2.2	V
				6.0	–	3.0	3.0	3.0	V
Hysteresis Voltage	V_H		Min	2.0	–	0.2	0.2	0.2	V
				4.5	–	0.4	0.4	0.4	V
				6.0	–	0.5	0.5	0.5	V
			Max	2.0	–	1.0	1.0	1.0	V
				4.5	–	1.4	1.4	1.4	V
				6.0	–	1.5	1.5	1.5	V
Minimum HIGH Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \leq 20\mu A$		2.0	2.0	1.9	1.9	1.9	V
				4.5	4.5	4.4	4.4	4.4	V
				6.0	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}	$\|I_{OUT}\| \leq$ 4.0mA	4.5	4.2	3.98	3.84	3.70	V
			$\|I_{OUT}\| \leq$ 5.2mA	6.0	5.7	5.48	5.34	5.20	V
Maximum LOW Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \leq 20\mu A$		2.0	0	0.1	0.1	0.1	V
				4.5	0	0.1	0.1	0.1	V
				6.0	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}	$\|I_{OUT}\| \leq$ 4.0mA	4.5	0.2	0.26	0.33	0.40	V
			$\|I_{OUT}\| \leq$ 5.2mA	6.0	0.2	0.26	0.33	0.40	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0µA		6.0	–	2.0	20	40	µA

Note 4. For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively (The V_{IH} value at 5.5V is 3.85V). The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics: (V_{CC} = 5V, $t_r = t_f$ = 6ns, C_L = 15pF, T_A = +25°C unless otherwise specified)

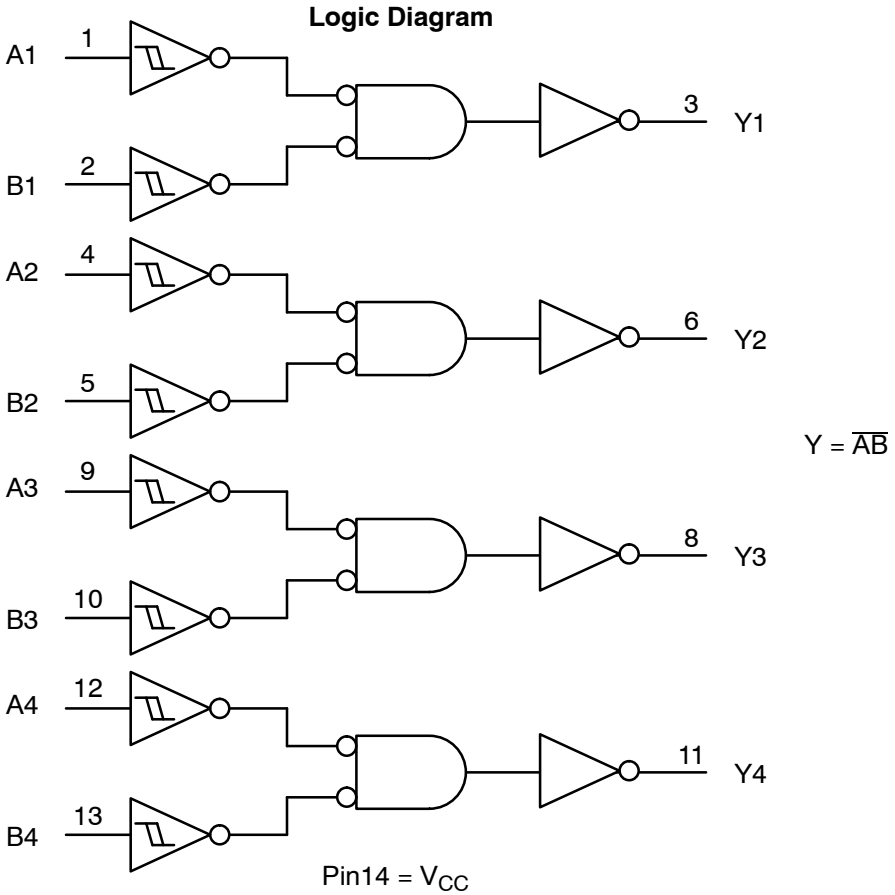
Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Maximum Propagation Delay	t_{PHL}, t_{PLH}		12	20	ns

AC Electrical Characteristics: (V_{CC} = 5V ±10%, $t_r = t_f$ = 6ns, C_L = 50pF unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C	−40° to +85°C	−40° to +125°C	Unit
				Typ	Guaranteed Limits		
Maximum Propagation Delay	t_{PHL}, t_{PLH}		2.0	63	125	158	186	V
			4.5	13	25	32	37	V
			6.0	11	21	27	32	V
Maximum Output Rise and Fall Time	t_{THL}, t_{TLH}		2.0	30	75	95	110	V
			4.5	8	15	19	22	V
			6.0	7	13	16	19	V
Power Dissipation Capacitance	C_{PD}	Per gate, Note 5	–	130	–	–	–	pF
Maximum Input Capacitance	C_{IN}		–	–	5	10	10	pF

Note 5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



Pin Connection Diagram