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NTE74HC10
Integrated Circuit
TTL – High Speed CMOS,
Triple, 3–Input NAND Gate

Description:

The NTE74HC10 is a triple, 3–input NAND gate in a 14–Lead plastic DIP type package that utilizes silicon gate CMOS technology to achieve operating speeds similar to LS–TTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LS–TTL loads.

Features:

- Buffered Inputs
- Typical Propagation Delay: 8ns (typ)
- Fanout (Over Temperature Range):
  Standard Outputs . . . . . 10 LS–TTL Loads
  Bus Driver Outputs . . . . . 15 LS–TTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LS–TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Maximum Junction Temperature, T_J . . . . . +150°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Typical Thermal Resistance, Junction–to–Ambient (Note 3), R_{thJA} . . . . . 100°C/W
Lead Temperature (During Soldering, 10sec), T_L . . . . . +300°C

Note 1. Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the Recommended Operating Conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the Recommended Operating Conditions may effect device reliability. The Absolute Maximum Ratings are stress ratings only.

Note 2. Unless otherwise specified, all voltages are referenced to GND.

Note 3. R_{thJA} is measured with the component mounted on an evaluation PC board in free air.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–55	–	+125	°C
Input Rise or Fall Times V_{CC} = 2.0V	t_r, t_f	–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics:

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			–40° to +85°C		–55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
High Level Input Voltage	V_{IH}		2.0	1.5	–	–	1.5	–	1.5	–	V
			4.5	3.15	–	–	3.15	–	3.15	–	V
			6.0	4.2	–	–	4.2	–	4.2	–	V
Low Level Input Voltage	V_{IH}		2.0	–	–	0.5	–	0.5	–	0.5	V
			4.5	–	–	1.35	–	1.35	–	1.35	V
			6.0	–	–	1.8	–	1.8	–	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IN} = V_{IH} or V_{IL}, I_O = –0.02mA	2.0	1.9	–	–	1.9	–	1.9	–	V
			4.5	4.4	–	–	4.4	–	4.4	–	V
			6.0	5.9	–	–	5.9	–	5.9	–	V
TTL Loads		V_I = V_{IH} or V_{IL}, I_O = –4mA	4.5	3.98	–	–	3.84	–	3.7	–	V
		V_I = V_{IH} or V_{IL}, I_O = –5.2mA	6.0	5.48	–	–	5.34	–	5.2	–	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IN} = V_{IH} or V_{IL}, I_O = 0.02mA	2.0	–	–	0.1	–	0.1	–	0.1	V
			4.5	–	–	0.1	–	0.1	–	0.1	V
			6.0	–	–	0.1	–	0.1	–	0.1	V
TTL Loads		V_{IN} = V_{IH} or V_{IL}, I_O = 4mA	4.5	–	–	0.26	–	0.33	–	0.4	V
		V_{IN} = V_{IH} or V_{IL}, I_O = –5.2mA	6.0	–	–	0.26	–	0.33	–	0.4	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND	6.0	–	–	±0.1	–	±1.0	–	±1.0	µA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_O = 0mA	6.0	–	–	2.0	–	20	–	40	µA

Switching Characteristics: (t_r = t_f = 6ns)

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			–40° to +85°C		–55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Propagation Delay, Input to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	–	100	–	125	–	150	ns
			4.5	–	–	20	–	25	–	30	ns
			6.0	–	–	17	–	21	–	26	ns
Propagation Delay, Data Input to Output Y	t_{PLH}, t_{PHL}	C_L = 15pF	5.0	–	8	–	–	–	–	–	ns

Switching Characteristics (Cont'd): ($t_r = t_f = 6ns$)

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			−40° to +85°C		−55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Transition Times	t_{TLH}, t_{THL}	C_L = 50pF	2.0	–	–	75	–	95	–	110	ns
			4.5	–	–	15	–	19	–	22	ns
			6.0	–	–	13	–	16	–	19	ns
Input Capacitance	C_{IN}		–	–	–	10	–	10	–	10	pF
Power Dissipation Capacitance	C_{PD}	Note 4	5	–	24	–	–	–	–	–	pF

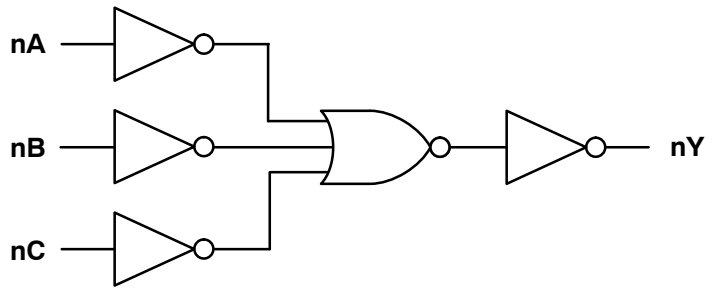
Note 4. C_{PD} is used to determine the dynamic power consumption, per gate. $P_D = V_{CC}^2 f_I (C_{PD} + C_L)$ where f_I = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Truth Table:

Inputs			Output
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

H = HIGH Level
L = LOW Level

Logic Diagram



Pin Connection Diagram