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## NTE74HC00 Integrated Circuit TTL – High Speed CMOS, Quad 2–Input NAND Gate

**Description:**

The NTE74HC00 is a NAND gate in a 14–Lead plastic DIP type package fabricated using advanced silicon–gate CMOS technology which provides the inherent benefits of CMOS – low quiescent power and wide power supply range. This device is input and output characteristic and pinout compatible with standard NTE74LS logic families. All inputs are protected from static discharge damage by internal diodes to  $V_{CC}$  and ground.

The NTE74HC00 is intended to interface between TTL and NMOS components and standard CMOS devices. This device is also a plug–in replacement for LS–TTL devices and can be used to reduce power consumption in existing designs.

**Absolute Maximum Ratings:** (Note 1, Note 2)

Supply Voltage, $V_{CC}$ .....	–0.5 to +7.0V
DC Input Voltage, $V_{IN}$ .....	–0.5 to $V_{CC} + 0.5V$
DC Output Voltage, $V_{OUT}$ .....	–0.5 to $V_{CC} + 0.5V$
DC Input Current (Per Pin), $I_{IN}$ .....	$\pm 20mA$
DC Output Current (Per Pin), $I_{OUT}$ .....	$\pm 25mA$
DC $V_{CC}$ or GND Current (Per Pin), $I_{CC}$ .....	$\pm 50mA$
Power Dissipation (Note 3), $P_D$ .....	600mW
Storage Temperature Range, $T_{stg}$ .....	–65°C to +150°C
Lead Temperature (During Soldering, 10sec), $T_L$ .....	+260°C

Note 1. Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the Recommended Operating Conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the Recommended Operating Conditions may effect device reliability. The Absolute Maximum Ratings are stress ratings only.

Note 2. Unless otherwise specified, all voltages are referenced to GND.

Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

### Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	2.0	–	6.0	V
DC Input or Output Voltage	$V_{IN}, V_{OUT}$	0	–	$V_{CC}$	V
Operating Temperature Range	$T_A$	–55	–	+125	°C
Input Rise or Fall Times $V_{CC} = 2.0V$	$t_r, t_f$	–	–	1000	ns
$V_{CC} = 4.5V$		–	–	500	ns
$V_{CC} = 6.0V$		–	–	400	ns

### DC Electrical Characteristics: ( $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Parameter	Symbol	Test Conditions	$V_{CC}$ (V)	Guaranteed Limits			Unit
				–55 to +25°C	≤ 85°C	≤ 125°C	
Minimum High Level Input Voltage	$V_{IH}$	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ , $ I_{OUT}  \leq 20\mu A$	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	V
			4.5	3.15	3.15	3.15	V
			6.0	4.20	4.20	4.20	V
Maximum Low Level Input Voltage	$V_{IH}$	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ , $ I_{OUT}  \leq 20\mu A$	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	V
			4.5	1.35	1.35	1.35	V
Minimum High Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$ , $ I_{OUT}  \leq 20\mu A$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	V
			6.0	5.9	5.9	5.9	V
	$V_{IN} = V_{IH}$ or $V_{IL}$	$ I_{OUT}  \leq 2.4mA$	3.0	2.48	2.34	2.20	V
			4.5	3.98	3.84	3.70	V
			6.0	5.48	5.34	5.20	V
Maximum Low Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$ , $ I_{OUT}  \leq 20\mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	V
			6.0	0.1	0.1	0.1	V
	$V_{IN} = V_{IH}$ or $V_{IL}$	$ I_{OUT}  \leq 2.4mA$	3.0	0.26	0.33	0.40	V
			4.5	0.26	0.33	0.40	V
			6.0	0.26	0.33	0.40	V
Maximum Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	6.0	2.0	20	40	μA

### AC Electrical Characteristics: ( $t_r = t_f = 6ns$ , $C_L = 15pF$ unless otherwise specified)

Parameter	Symbol	Test Conditions	$V_{CC}$ (V)	Guaranteed Limits			Unit
				–55 to +25°C	≤ 85°C	≤ 125°C	
Maximum Propagation Delay, Input A or B to Output Y	$t_{PLH}$ , $t_{PHL}$		2.0	75	95	110	ns
			3.0	30	40	55	ns
			4.5	15	19	22	ns
			6.0	13	16	19	ns

**AC Electrical Characteristics (Cont'd):** ( $t_r = t_f = 6\text{ns}$ ,  $C_L = 15\text{pF}$  unless otherwise specified)

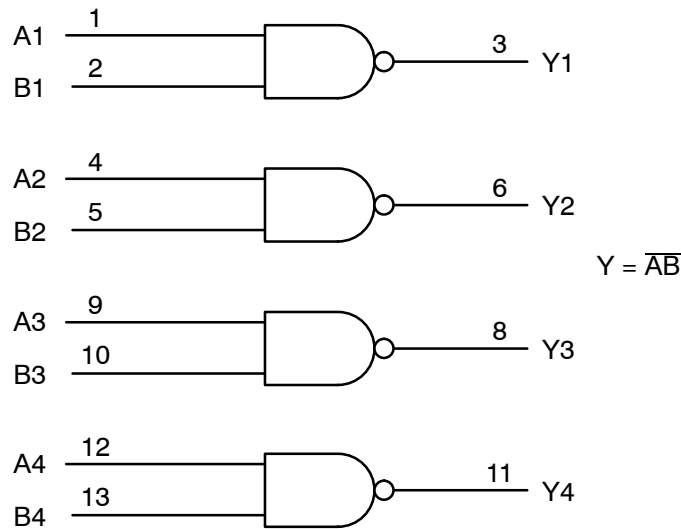
Parameter	Symbol	Test Conditions	V <sub>CC</sub> (V)	Guaranteed Limits			Unit
				-55 to +25°C	≤ 85°C	≤ 125°C	
Maximum Output Transition Time, Any Output	t <sub>TLH</sub> , t <sub>THL</sub>		2.0	75	95	110	ns
			3.0	27	32	36	ns
			4.5	15	19	22	ns
			6.0	13	16	19	ns
Maximum Input Capacitance	C <sub>in</sub>		-	10	10	10	pF
Parameter	Symbol	Test Conditions	Typical @ +25°C, V <sub>CC</sub> = 5V, V <sub>EE</sub> = 0V			Unit	
Power Dissipation Capacitance (Per Buffer)	C <sub>PD</sub>	Note 4	22			pF	

Note 4. C<sub>PD</sub> determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

**Truth Table:**

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

**Logic Diagram**



Pin14 = V<sub>CC</sub>  
Pin7 = GND

### Pin Connection Diagram

