ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE74393
Integrated Circuit
TTL – Dual 4–Bit Binary Ripple Counter

Description:

The NTE74393 is a monolithic dual 4–bit binary ripple counter in a 14–Lead plastic DIP type package that contains eight master–slave flip–flops and additional gating to implement two individual four–bit counters. This device contains two independent four–bit binary counters each having a clear and a clock input. N–bit binary counters can be implemented with each package providing the capability of divide–by–265.

The NTE74393 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system–timing signals.

Features:

- Dual,Version of the Popular NTE7493
- Dual 4–Bit Binary Counter with Individual Clocks
- Direct Clear for each 4–Bit Counter
- Dual 4–Bit Versions can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency: 35Mhz
- Buffered Outputs Reduce Possibility of Collector Commutation

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	−800	μA
Low−Level Output Current	I_{OL}	–	–	16	mA
Count Frequency A Input	f_{count}	0	–	25	MHz
B Input		0	–	20	MHz
Pulse Width A Input High or Low	t_w	20	–	–	ns
B Input High or Low		25	–	–	ns
Clear High		20	–	–	ns
Clear Inactive−State Setup Time (Note 2)	t_{su}	25↓	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Note 2. .The arrow indicates that the falling edge of the clock pulse is used for reference.

Electrical Characteristics: (Note 3, Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2	–	–	V
Low Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA	2.4	3.4		V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA, Note 5	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current Clear	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	40	μA
Input A			–	–	80	μA
Low Level Input Current Clear	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−1	mA
Input A			–	–	−3.2	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 6	−18	–	−57	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 7	–	38	64	mA

Note 3. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 4. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 5. The Q_A outputs are tested at I_{OL} = 16mA plus the limit value for I_{IL} for the clock B input. This permits driving the clock B input while maintaining full fan−out capability

Note 6. Not more than one output should be shorted at a time.

Note 7. I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Count Frequency (From A Input to Q_A Output)	f_{max}	R_L = 400Ω, C_L = 15pF	25	35	–	MHz
Propagation Delay Time (From A input to Q_A Output)	t_{PLH}		–	12	20	ns
	t_{PHL}		–	13	20	ns
Propagation Delay Time (From A input to Q_D Output)	t_{PLH}		–	40	60	ns
	t_{PHL}		–	40	60	ns
Propagation Delay Time (From Clear input to Any Output)	t_{PHL}		–	24	39	ns

Function Table:

Count Sequence (Each Counter):

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

Pin Connection Diagram