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NTE74191
Integrated Circuit
TTL − Synchronous Up/Down Counter

Description:

The NTE74191 is a synchronous 4−bit binary reversible up/down counter in a 16−Lead plastic DIP type package having the complexity of 58 equivalent gates. Synchronous operation is provided by having all flip−flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master−slave flip−flops are triggered on a low−to−high transition of the clock input if the enable input is low, A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

This counter is fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at th data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo−N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high−level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low−level output pulse equal in width to the low−level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look−ahead for high−speed operation.

Features:

- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presettable with Load Control
- Parallel Outputs
- Cascadable for n−Bit Applications

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} . . . 7V
DC Input Voltage, V_{IN} . . . 5.5V
Power Dissipation, P_D . . . 325mW
Operating Temperature Range, T_A . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . −65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	−0.8	mA
Low−Level Output Current	I_{OL}	–	–	16	mA
Clock Frequency	f_{clock}	0	–	20	MHz
Width of Clock Input Pulse	$t_{w(clock)}$	25	–	–	ns
Width of Load Input Pulse	$t_{w(load)}$	35	–	–	ns
Data Setup Time	t_{su}	20	–	–	ns
Load Inactive Setup Time	t_{su}	20	–	–	ns
Data Hold Time	t_h	0	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

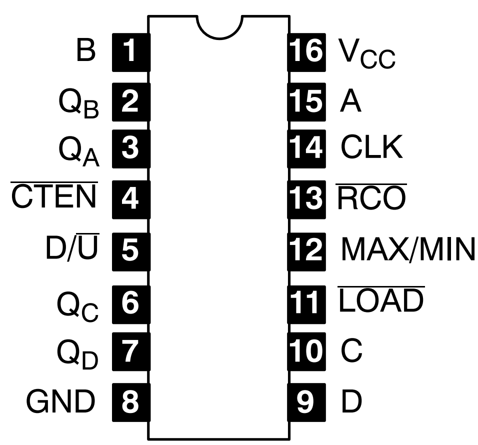
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}			2	–	–	V
Low−Level Input Voltage	V_{IL}			–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA		–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −0.8mA		2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA		–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V		–	–	1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.4V	Enable	–	–	120	μA
			Others	–	–	40	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	Enable	–	–	−4.8	mA
			Others	–	–	−1.6	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 5		−18	–	−65	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 6		–	65	105	mA

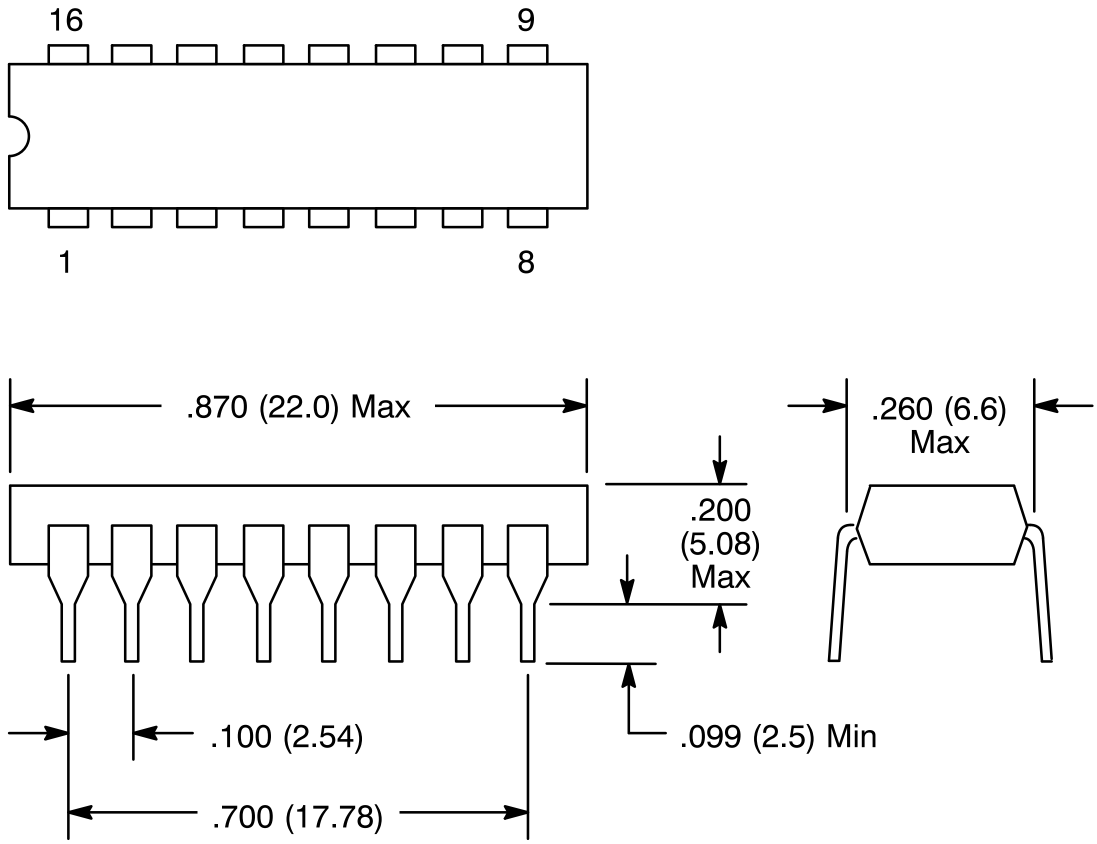
Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.
Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.
Note 4. Not more than one output should be shorted at a time.
Note 5. I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 400Ω, C_L = 15pF	20	25	–	MHz
Propagation Delay Time (From $\overline{\text{Load}}$ Input to Any Q Output)	t_{PLH}		–	22	33	ns
	t_{PHL}		–	33	50	ns
Propagation Delay Time (From Any Data Input to Any Q Output)	t_{PLH}		–	14	22	ns
	t_{PHL}		–	35	50	ns
Propagation Delay Time (From CLK Input to $\overline{\text{RCO}}$ Output)	t_{PLH}		–	13	20	ns
	t_{PHL}		–	16	24	ns
Propagation Delay Time (From Clock Input to Any Q Output)	t_{PLH}		–	16	24	ns
	t_{PHL}		–	24	36	ns
Propagation Delay Time (From Clock Input to Max/Min Output)	t_{PLH}		–	28	42	ns
	t_{PHL}		–	37	52	ns
Propagation Delay Time (From D/$\overline{\text{U}}$ Input to $\overline{\text{RCO}}$ Output)	t_{PLH}		–	30	45	ns
	t_{PHL}		–	30	45	ns
Propagation Delay Time (From D/$\overline{\text{U}}$ Input to Max/Min Output)	t_{PLH}		–	21	33	ns
	t_{PHL}		–	22	33	ns

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6) Max
.200 (5.08) Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)