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NTE74156 Integrated Circuit TTL – Dual 2–Line–to–1–Line Decoder/Demultiplexer

Description:

The NTE74156 is a monolithic TTL circuit featuring dual 1–line–to–4–line demultiplexers with individual strobes and common binary–address inputs in a 16–Lead plastic DIP type package. When both sections are enabled by the strobes, the common binary–address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4–bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at $2\bar{C}$ is not inverted through its outputs. The inverter following the 1C data input permits use as a 3–to–8–line decoder or 1–to–8–line demultiplexer without external gating. Input clamping diodes are provided on all of the circuits to minimize transmission–line effects and simplify system design.

Features:

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Input Clamping Diodes Simplify System Design
- Open Collector Outputs

Applications:

- Dual 2–to–4–Line Decoder
- Dual 1–to–4–Line Demultiplexer
- 3–to–8–Line Decoder
- 1–to–8–Line Demultiplexer

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC}	7V
DC Input Voltage, V_{IN}	5.5V
Off–State Voltage	5.5V
Power Dissipation, P_D	125mW
Operating Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_{stg}	–65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Output Voltage	V_{OH}	–	–	5.5	V
Low–Level Output Current	I_{OL}	–	–	16	mA
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2	-	-	V
Low Level Input Voltage	V_{IL}		-	-	0.8	V
Input Clamp Voltage	V_{IK}	$V_{CC} = \text{MIN}, I_I = -8\text{mA}$	-	-	-1.5	V
High Level Output Current	I_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, V_{OH} = 5.5\text{V}$	-	-	250	μA
Low Level Output Voltage	V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OL} = 16\text{mA}$	-	0.2	0.4	V
Input Current	I_I	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$	-	-	1	mA
High Level Input Current	I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$	-	-	40	μA
Low Level Input Current	I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$	-	-	-1.6	mA
Supply Current	I_{CC}	$V_{CC} = \text{MAX}, \text{Note 4}$	-	25	40	mA

Note 2. For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

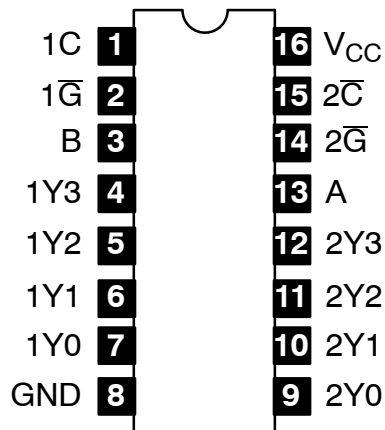
Note 3. All typical values are at $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$.

Note 4. I_{CC} is measured with the outputs open, A, B, and 1C inputs at 4.5V, and 2C, 1G, and 2G inputs grounded.

Switching Characteristics: ($V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Levels of Logic	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From A, B, 2C, 1G or 2G Input to Y Output)	t_{PLH}	2	$R_L = 400\Omega,$ $C_L = 15\text{pF}$	-	15	23	ns
	t_{PHL}	2		-	20	30	ns
Propagation Delay Time (From A or B Input to Y Output)	t_{PLH}	3		-	23	34	ns
	t_{PHL}	3		-	23	34	ns
Propagation Delay Time (From 1C Input to Y Output)	t_{PLH}	3		-	18	27	ns
	t_{PHL}	3		-	22	33	ns

Pin Connection Diagram



Function Tables:

2-Line-to-4-Line Decoder
or 1-Line-to-4-Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data	1Y0	1Y1	1Y2	1Y3
B	A	\overline{G}	1C				
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data	2Y0	2Y1	2Y2	2Y3
B	A	$2\overline{G}$	$2\overline{C}$				
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

Function Table:

3-Line-to-8-Line Decoder
or 1-Line-to-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C *	B	A	\overline{G} **	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

* C = Inputs 1C and $2\overline{C}$ connected together

** \overline{G} = Inputs $1\overline{G}$ and $2\overline{G}$ connected together

H = HIGH Level

L = LOW Level

X = Don't Care

