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NTE74116 Integrated Circuit TTL – Dual 4–Bit Latch with Clear

Description:

The NTE74116 is a monolithic dual 4-bit latch in a 24-Lead plastic DIP type package that utilizes D-type bistables to implement two independent four-bit latches. Each four-bit latch has an independent asynchronous clear input and a gated two-input enable circuit. When both enable inputs are low, the output levels will follow the data input levels. When either or both of the enable inputs are taken high, the outputs remain at the last levels setup at the inputs prior to the low-to-high transition at the enable input(s). After this, the data inputs are locked out.

The clear input is overriding and when taken low will reset all four outputs low regardless of the levels of the enable inputs.

Features:

- Two Independent 4–Bit Latches in a Single Package
- Separate Clear Inputs Provide One–Step Clearing Operation
- Dual Gated Enable Inputs Simplify Cascading Register Implementations
- Input Clamping Diodes Simplify System Design

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
 DC Input Voltage, V_{IN} 5.5V
 Operating Temperature Range, T_A 0°C to +70°C
 Storage Temperature Range, T_{stg} –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Output Current	I_{OH}	–	–	–800	μA
Low–Level Output Current	I_{OL}	–	–	16	mA
Input Pulse Width C1, C2	t_w	18	–	–	ns
\overline{PRE} or \overline{CLR} Low		18	–	–	ns
Data Setup Time High Logic Level	t_{su}	8	–	–	ns
Low Logic Level		14	–	–	ns
Other Inactive–State Setup Time	t_{su}	8	–	–	ns
Data Release Time, High–Level Data	$t_{release}$	–	–	2	ns
Data Hold Time, Low–Level Data	t_h	8	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
High-Level Input Voltage	V_{IH}		2	-	-	V	
Low-Level Input Voltage	V_{IL}		-	-	0.8	V	
Input Clamp Voltage	V_{IK}	$V_{CC} = \text{MIN}, I_I = -12\text{mA}$	-	-	-1.5	V	
High Level Output Voltage	V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = -800\mu\text{A}$	2.4	3.4	-	V	
Low Level Output Voltage	V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OL} = 16\text{mA}$	-	0.2	0.4	V	
Input Current	I_I	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$	-	-	1	mA	
High Level Input Current $\overline{C}1, \overline{C}2, \text{ or Clear}$	I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$	-	-	40	μA	
Any D			-	-	60	μA	
Low Level Input Current $\overline{C}1, \overline{C}2, \text{ or Clear}$	I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$	-	-	-1.6	mA	
Any D, Initial Peak			-	-	-2.4	mA	
Any D, Steady-State			-	-	-1.6	mA	
Short-Circuit Output Current	I_{OS}	$V_{CC} = \text{MAX}, \text{ Note 4}$	-18	-	-57	mA	
Supply Current	I_{CC}	$V_{CC} = \text{MAX}, \text{ Note 5}$	Condition A	-	60	100	mA
			Condition B	-	40	70	mA

Note 2. For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 3. All typical values are at $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$.

Note 4. Not more than one output should be shorted at a time.

Note 5. With outputs open, I_{CC} is measured for the following conditions:

A. All outputs grounded.

B. All \overline{C} inputs are grounded and all other inputs are at 4.5V.

Switching Characteristics: ($V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From $\overline{C}1$ or $\overline{C}2$ Input to Any Q Output)	t_{PLH}	$R_L = 400\Omega, C_L = 15\text{pF}$	-	19	30	ns
	t_{PLH}		-	15	22	ns
Propagation Delay Time (From Data Input to Q Output)	t_{PLH}		-	10	15	ns
	t_{PLH}		-	12	18	ns
Propagation Delay Time (From \overline{CLR} Input to Any Q Output)	t_{PHL}		-	15	22	ns

Function Table (Each Latch):

Inputs			Data	Output Q
$\overline{\text{Clear}}$	Enable			
	$\overline{C}1$	$\overline{C}2$		
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Q_0
H	H	X	X	Q_0
L	X	X	X	L

H = High Level, L = Low Level, X = Irrelevant

Q_0 = The level of Q before these input conditions were established

Pin Connection Diagram

