ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE7196
Integrated Circuit
H–Bridge with Motor Control

Description:

The NTE7196 is a 3A H–Bridge in an 11–Lead Staggered SIP type package designed for motion control applications. The device is built using a multi–technology process which combines bipolar and CMOS control circuitry with DMOS power devices on the same monolithic structure. The H–Bridge configuration is ideal for driving DC and stepper motors. The NTE7196 accommodates peak output currents up to 6A. Current sensing can be achieved via a small sense resistor connected in series with the power ground lead. For current sensing without disturbing the path of current to the load, the NTE7196 is recommended.

Features:

- Delivers up to 3A Continuous Output
- Operates at Supply Voltages up to 55V
- Low $R_{DS(ON)}$ Typically 0.33Ω per Switch
- TTL and CMOS Compatible Inputs
- No “Shoot–Through” Current
- Thermal Warning Flag Output at +145°C
- Thermal Shutdown (Outputs off) at +170°C
- Internal Clamp Diodes
- Shorted Load Protection
- Internal Charge Pump w/External Bootstrap Capability

Applications:

- DC and Stepper Motor Drives
- Position and Velocity Servomechanisms
- Factory Automation Robots
- Numerically Controlled Machinery
- Computer Printers and Plotters

Absolute Maximun Ratings: (Note 1)

Total Supply Voltage (V_S, Pin6) 60V
Voltage at Pins 3, 4, 5, and 9 . . . . . 12V
Voltage at Bootstrap Pins (Pin1 and Pin11) . . . . . V_{OUT} + 16V
Peak Output Current (200ms) 6A
Continuous Output Current 3A
Power Dissipation (Note 2) 25W
Sense Voltage (Pin7 to Pin8) . . . . . +0.5V to –1.0V
Power Dissipation (T_A= +25°C, Free Air) 3W
Junction Temperature, $T_{J(max)}$ . . . . . 150°C
ESD Susceptibility (Note 3) 1500V
Storage Temperature, T_{STG} . . . . . –40° to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Note 1. Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions

Note 2. The maximum power dissipation must be derated at elevated temperatures and is a function of $T_{J(max)}$, $R_{thJA,}$ and T_A. The maximum allowable power dissipation at any temperature is $P_{D(max)} = (T_{J(max)} - T_A)/R_{thJA,}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The typical thermal resistance from junction to case (R_{thJC}) is 1.0°C/W and from junction to ambient (R_{thJA}) is 30°C/W. For guaranteed operation $T_{J(max)}$ = +125°C.

Note 3. Human−Body model, 100 pF discharged through a 1.5 kΩ resistor. Except Bootstrap pins (pins 1 and 11) which are protected to 1000V of ESD

Recommended Operating Conditions: (Note 1)

Junction Temperature, T_J ..... _40° to +125°C

V_S Supply Voltage ..... +12V to +55V

Note 1 Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions

Electrical Characteristics: (V_s = 42V, $T_A = T_J$ = +25°C, Note 5, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Switch ON Resistance	$R_{DS(ON)}$	I_O = 3A, Note 5		−	0.33	0.4	Ω
Switch ON Resistance	$R_{DS(ON)}$		−40° ≤ T_j ≤ +125°C	−	0.33	0.6	Ω
Switch ON Resistance	$R_{DS(ON)}$	I_O = 6A, Note 5		−	0.33	0.4	Ω
Switch ON Resistance	$R_{DS(ON)}$		−40° ≤ T_j ≤ +125°C	−	0.33	0.6	Ω
Clamp Diode Forward Drop	V_{CLAMP}	Clamp Current = 3A, Note 5		−	1.2	.5	V
Logic Low Input Voltage	V_{IL}	Pins 3, 4, 5		−	−	−0.10	V
Logic Low Input Voltage	V_{IL}		−40° ≤ T_j ≤ +125°C	−	−	0.8	V
Logic Low input Current	I_{IL}	V_{IN} = −0.1V, Pincs = 3, 4, 5 , −40° ≤ T_j ≤ +125°C		−	−	−10	μA
Logic High Input Voltage	V_{IH}	Pins 3, 4, 5, −40° ≤ T_j ≤ +125°C		2	−	12	V
Logic High Input Current	I_{IL}	V_{IN} = 12V, Pins 3, 4, 5		−	−	10	μA
Undervoltage Lockout		Outputs Turn OFF		9	−	11	V
Warning Flag Temperature	T_{JW}	Pin 9 ≤ 0.8V, I_L = 2 mA		−	145	−	°C
Flag Output Saturation Voltage	$V_{F(ON)}$	$T_J = T_{JW}$, I_L = 2 mA		−	0.15	−	V
Flag Output Leakage	$I_{F(OFF)}$	V_F = 12V		−	0.2	10	μA
Shutdown Temperature	T_{JSD}	Outputs Turn Off		−	170	−	°C
Quiescent Supply Current	I_S	All Logic Inputs Low		−	13	25	mA
Output Turn−On Delay Time	$t_{D(ON)}$	Sourcing Outputs, I_{OUT} = 3A		−	300	−	ns
		Sinking Outputs, I_{OUT} = 3A		−	300	−	ns
Output Turn−On Switching Time	t_{ON}	Bootstrap Capacitor = 10 nF	Sourcing Outputs, I_{OUT} = 3A	−	100	−	ns
			Sinking Outputs, I_{OUT} = 3A	−	80	−	ns
Output Turn−Off Delay Times	$T_{D(OFF)}$	Sourcing Outputs, I_{OUT} = 3A		−	200	−	ns
		Sinking Outputs, I_{OUT} = 3A		−	200	−	ns

Note 4. All limits are 100% production tested at +25°C. Temperature extreme limits are guaranteed via correlation using accepted SQC (Statistical Quality control) methods. All limits are used to calculate AOQL, (Average Outgoing Quality Level).

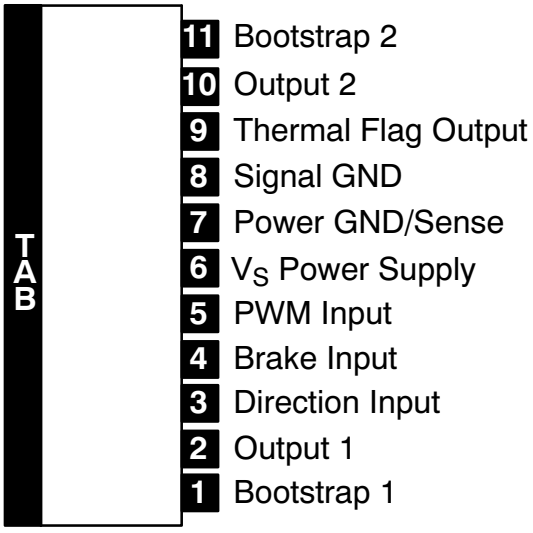
Note 5. Output currents are pulsed (t_W < 2 ms, Duty Cycle < 5%).

Electrical Characteristics (Cont'd): (V_S = 42V, $T_A = T_J$ = +25°C, Note 4, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Turn–Off Switching Times	t_{OFF}	Bootstrap Capacitor = 10 nF	Sourcing Outputs, I_{OUT} = 3A	–	75	–	ns
			Sinking Outputs, I_{OUT} = 3A	–	70	–	ns
Minimum Input Pulse Width	t_{PW}	Pins 3, 4, and 5		–	1	–	μs
Charge Pump Rise Time	t_{CPR}	No Bootstrap Capacitor		–	20	–	μs

Note 4 All limits are 100% production tested at +25°C. Temperature extreme limits are guaranteed via correlation using accepted SQC (Statistical Quality control) methods. All limits are used to calculate AOQL, (Average Outgoing Quality Level).

Pin Connection Diagram
(Front View)



Note: Tab connected to Pin7.