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NTE7162
Integrated Circuit
DC−Coupled Vertical Deflection and East−West Output Circuit

Description:

The NTE7162 is a power circuit in a 13−Lead Staggered SIP type package designed for use in 90° and 110° color deflection systems for field frequencies of 50Hz to 120Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly effecient class G system and an East−West driver for sinking the diode modulator current.

Features:

- Few External Components
- Highly Efficient Fully DC−Coupled Vertical Output Bridge Circuit
- Vertical Flyback Switch
- Guard Circuit
- Protection Against:
  - Short−Circuit of the Output Pins
  - Short−Circuit of the Output Pins to V_P
- High EMC Immunity due to Common Mode Inputs
- Temperature Protectection
- East−West Output Stge with One Single Conversion Resistor

Absolute Maximum Ratings:

Supply Voltage, V_P
- Operating 25V
- Non−Operating 40V

Flyback Supply Voltage, V_{FB} 50V
Flyback Supply Voltage (Note 1), V_{FB} 60V
Output Current (Peak−to−Peak Value, Note 2), I_O 3A
Output Voltage (Pin9), $V_{O(A)}$ 52V
Output Voltage (Pin9, Note 1), $V_{O(A)}$ 52V
Peak Output Current, I_M . . . . ±1.5A
Output Voltage ($I_{O(sink)}$ = 10µA, Note 3), $V_{O(sink)}$ 40V
Output Current ($V_{O(sink)}$ = 2V, Note 3), $I_{O(sink)}$ 500mA

Note 1. A flyback supply voltage of > 50V up to 60V i allowed in application. A 220nF capacitor in series with a 22Ω resistor (depending on I_O and the inductance of the coil) has to be connected between Pin9 and GND. The decoupling capacitor of V_{FB} has to be connected between Pin8 and Pin4. The supply voltage line must have a resistance of 33Ω.

Note 2. I_O maximum determined by current protection.

Note 3. The operating area is limited by a straight line between the points $V_{O(sink)}$ = 40V; $I_{O(sink)}$ = 10µA and $V_{O(sink)}$ = 2V; $I_{O(sink)}$ = 500mA.

Absolute Maximum Ratings (Cont'd):

Virtual Junction Temperature, T_{VJ} . . . . +150°C
Operating Ambient Temperature Range, T_A . . . . −25° to +75°C
Storage Temperature Range, T_{stg} . . . . −65° to +150°C
Thermal Resistance, Virtual Junction−to−Case, R_{thVJC} 4K/W
Thermal Resistance, Virtual Junction−to−Ambient (In Free Air), R_{thVJA} 40K/W
Short−Circuiting Time (Note 4), t_{sc} . . . . 1 Hour

Note 4. Up to V_P = 10V.

Electrical Characteristics: (V_P = 17.5V, V_{FB} = 45V, $V_{O(sink)}$ = 20V, f_i = 50Hz, $I_{I(sb)}$ = 400μA, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Supply						
Operating Supply Voltage	V_P		9	−	25	V
Flyback Supply Voltage	V_{FB}		V_P	−	50	V
		Note 1	−	−	60	V
Supply Current	I_P	No Signal, No Load	−	30	55	mA
Vertical Circuit						
Output Voltage Swing (Scan)	V_O	I_{diff} = 0.6mA (Peak−to−Peak), V_{diff} = 1.8V (Peak−to−Peak), I_O = 3A (Peak−to−Peak)	19.8	−	−	V
Linearity Error	LE	I_O = 3A (Peak−to−Peak), Note 5	−	1	3	%
		I_O = 50mA (Peak−to−Peak), Note 5	−	1	3	%
Output Voltage Swing (Flyback) $V_{O(A)} - V_{O(B)}$	V_O	I_{diff} = 0.3mA, I_O = 1.5A	−	39	−	V
Forward Voltage of the Internal Effeciency Diode ($V_{O(A)} - V_{FB}$)	V_{DF}	I_O = −1.5A, I_{diff} = 0.3mA	−	−	1.5	V
Output Offset Current	$\|I_{OS}\|$	I_{diff} = 0, $I_{I(sb)}$ = 50μA to 500μA	−	−	30	mA
Offset Voltage at the Input of the Feedback Amplifier $V_{I(fb)} = V_{O(B)}$	$\|V_{OS}\|$	I_{diff} = 0, $I_{I(sb)}$ = 50μA to 500μA	−	−	18	mV
Output Offset Voltag as a Function of Temperature	ΔV_{OS} T	I_{diff} = 0	−	−	72	μV/K
DC Output Voltage	$V_{O(A)}$	I_{diff} = 0, Note 6	−	8	−	V
Open Loop Voltage Gain V_{9-5}/V_{1-2}	G_V	Note 7, Note 8	−	80	−	dB
V_{9-5}/V_{3-5}, V_{1-2} = 0		Note 7	−	80	−	dB

Note 1. A flyback supply voltage of > 50V up to 60V i allowed in application. A 220nF capacitor in series with a 22Ω resistor (depending on I_O and the inductance of the coil) has to be connected between Pin9 and GND. The decoupling capacitor of V_{FB} has to be connected between Pin8 and Pin4. The supply voltage line must have a resistance of 33Ω.

Note 5. The linearity error is measured without S−correction and based on the same measurement priinciple as performed on the screen. The measuring method is as follows:
Divide the output signal $I_5 - I_9$ (V_{RM}) into 22 equal parts ranging from 1 to 22 inclusive. measure the value of two succeeding parts called one block starting with 2 and 3 (block 1) and ending with 20 an 21 (block 10). Thus part 1 and 22 are unused. The equations for lineariy error for adjacent blocks (LEAB) and linearity error for not adjacent blocks (LENAB) are given below:

$$\text{LEAB} = \frac{a_k - a_{(k+1)}}{a_{avg}}\ ;\ \text{LENAB} = \frac{a_{max} - a_{min}}{a_{avg}}$$

Note 6. Referenced to V_P.

Note 7. The V values within formulae relate to voltages at or across the relative pin numbers, i.e. V_{9-5}/V_{1-2} = voltage value across Pin9 and Pin5 divided by voltage value across Pin1 and Pin2.

Note 8. V_{3-5} AC short−circuited.

Electrical Characteristics Cont'd): (V_P = 17.5V, V_{FB} = 45V, $V_{O(sink)}$ = 20V, f_i = 50Hz, $I_{I(sb)}$ = 400μA, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Ratio V_{1-2}/V_{3-5}	V_R		−	0	−	dB
Frequency Response (−3dB)	f_{res}	Note 9	−	40	−	Hz
Current Gain (I_O/I_{diff})	G_I		−	5000	−	
Current Gain as a Function of Temperature	ΔG_I T		−	−	10^{-4}	/K
Signal Bias Current	$I_{I(sb)}$		50	400	500	μA
Flyback Supply Current	I_{FB}	During Scan	−	−	100	μA
Power Supply Ripple Rejection	PSRR	Note 10	−	80	−	dB
DC Voltage at the Input	$V_{I(DC)}$		−	2.7	−	V
Common Mode Input Voltage	$V_{I(CM)}$	$I_{I(sb)}$ = 0	0	−	1.6	V
Input Bias Current	I_{bias}	$I_{I(sb)}$ = 0	−	0.1	0.5	μA
Common Mode Output Current	$I_{O(CM)}$	$\Delta I_{I(sb)}$ = 300μA (Peak−to−Peak), f_i = 50Hz, I_{diff} = 0	−	0.2	−	mA
East−West Amplifier						
Saturation Voltage	$V_{O(sink)}$	$I_{O(sink)}$ = 500mA, $I_{I(corr)}$ = 0μA, Note 11	−	2.0	2.5	V
Open Loop Voltage Gain (V_{11}/V_{12})	G_V		−	47	−	dB
Frequency Response (−3dB)	f_{res}		−	4000	−	Hz
Linearity Error	LE	$V_{O(sink)}$ = 3V	−	−	1	%
		$V_{O(sink)}$ = 10V, Note 5	−	−	0.5	%
Input Bias Current (Pin12)	I_{bias}		−	−	2	μA
DC Input Voltage	$V_{I(DC)}$		−	1	−	V
Offset Voltage Set Current	I_{set}		−	1	−	mA
Maximum Allowed Voltage at Pin13	V_{13-7}		−	−	0.3	V
Guard Circuit						
Output Current	I_O	Not Active, $V_{O(guard)}$ = 0V	−	−	50	μA
		Active, $V_{O(guard)}$ = 3.6V	1.0	−	2.5	mA
Output Voltage	$V_{O(guard)}$	I_O = 100μA	4.6	−	5.5	V
Allowable Voltage on Pin10		Maximum Leakage Current = 10μA	−	−	40	V

Note 5. The linearity error is measured without S−correction and based on the same measurement priinciple as performed on the screen. The measuring method is as follows:
Divide the output signal $I_5 - I_9$ (V_{RM}) into 22 equal parts ranging from 1 to 22 inclusive. measure the value of two succeeding parts called one block starting with 2 and 3 (block 1) and ending with 20 an 21 (block 10). Thus part 1 and 22 are unused. The equations forleariy error for adjacent blocks (LEAB) and linearity error for not adjacent blocks (LENAB) are given below:

$$LEAB = \frac{a_k - a_{(k+1)}}{a_{avg}} ; LENAB = \frac{a_{max} - a_{min}}{a_{avg}}$$

Note 9. Frequency response V_{9-5}/V_{3-5} is equal to frequency response V_{9-5}/V_{1-2}.
Note 10. At $V_{(ripple)}$ = 500mV eff; measured across R_M; f_i = 50Hz.
Note 11. The output Pin11 requires a capacitor with a minimum value of 68nF.

Pin Connection Diagram
(Front View)