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NTE4508B
Integrated Circuit
CMOS, Dual 4–Bit Latch

Description:

The NTE4508B is a dual 4–bit latch in a 24–Lead DIP type package constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. The part consists of two identical, independent 4–bit latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high impedance state and allow the devices to be used in time sharing bus line applications.

These complementary MOS latches find primary use in buffer storage, holding register, or general digital logic functions where low power dissipation and/or high noise immunity is desired.

Features:

- High Fanout > 50
- Input Impedance = 10^{12} Ohms (Typ)
- 3–State Output
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V9in9 and V9out9 be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 4) “0” Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	mAdc
(V_{OH} = 9.5Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	mAdc
(V_{OH} = 13.5Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	μAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	μAdc
		15	–	20	–	0.015	20	–	600	μAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 3, Note 5)	I_T	5.0	I_T = (1.46μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.91μA/kHz) f + I_{DD}							μAdc
		15	I_T = (4.37μA/kHz) f + I_{DD}							μAdc
Three State Leakage Current	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both “1” and “0” = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 8 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					
t_{TLH} = (3.0ns/pf) C_L + 30ns		5.0	–	180	360	ns
t_{TLH} = (1.5ns/pf) C_L + 15ns		10	–	90	180	ns
t_{TLH} = (1.1ns/pf) C_L + 10ns		15	–	65	130	ns
Output Fall Time	t_{THL}					
t_{THL} = (1.5ns/pf) C_L + 25ns		5.0	–	100	200	ns
t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 135ns		5.0	–	220	440	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 57ns		10	–	90	180	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 35ns		15	–	60	120	ns
Master Reset Pulse Width	$t_{WH(R)}$	5.0	200	100	–	ns
		10	100	50	–	ns
		15	70	35	–	ns
Strobe Pulse Width	$t_{WH(S)}$	5.0	140	70	–	ns
		10	70	35	–	ns
		15	40	20	–	ns
Setup Time	t_{su}	5.0	50	25	–	ns
		10	20	10	–	ns
		15	10	5	–	ns
Hold Time	t_h	5.0	0	0	–	ns
		10	0	0	–	ns
		15	0	0	–	ns
3−State Propagation Delay, Output “1” to High Impedance	t_{PHZ}					
t_{PHZ} = (0.49ns/pF) C_L + 60.5ns		5.0	–	85	170	ns
t_{PHZ} = (0.29ns/pF) C_L + 35.5ns		10	–	50	100	ns
t_{PHZ} = (0.19ns/pF) C_L + 25.5ns		15	–	35	70	ns
3−State Propagation Delay, High Impedance to Output “1”	t_{PZH}					
t_{PZH} = (0.41ns/pF) C_L + 64.5ns		5.0	–	85	170	ns
t_{PZH} = (0.31ns/pF) C_L + 34.5ns		10	–	50	100	ns
t_{PZH} = (0.30ns/pF) C_L + 20ns		15	–	35	70	ns
3−State Propagation Delay, Output “0” to High Impedance	t_{PLZ}					
t_{PLZ} = (0.32ns/pF) C_L + 49ns		5.0	–	65	130	ns
t_{PLZ} = (0.29ns/pF) C_L + 25.5ns		10	–	40	80	ns
t_{PLZ} = (0.28ns/pF) C_L + 16ns		15	–	30	60	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Switching Characteristics (Cont'd): (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
3−State Propagation Delay, High Impedance to Output "0" t_{PZL} = (0.49ns/pF) C_L + 60.5ns	t_{PZL}	5.0	–	85	170	ns
t_{PZL} = (0.29ns/pF) C_L + 35.5ns		10	–	50	100	ns
t_{PZL} = (0.19ns/pF) C_L + 25.5ns		15	–	35	70	ns

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

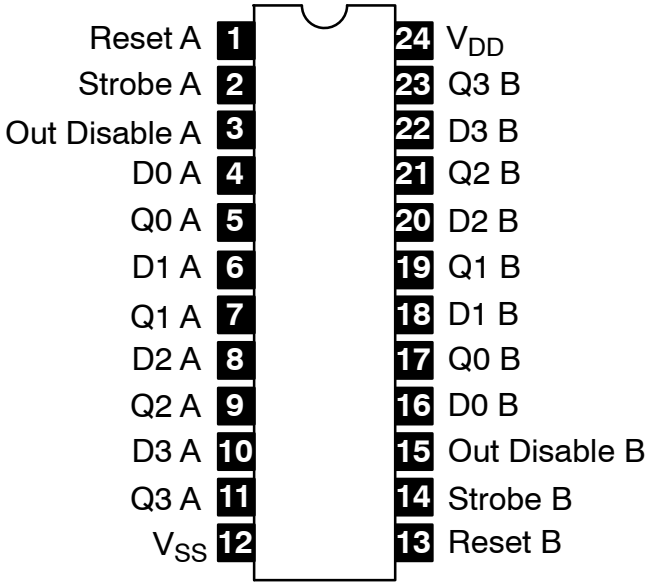
Note 3. The formulas given are for the typical characteristics only at +25°C.

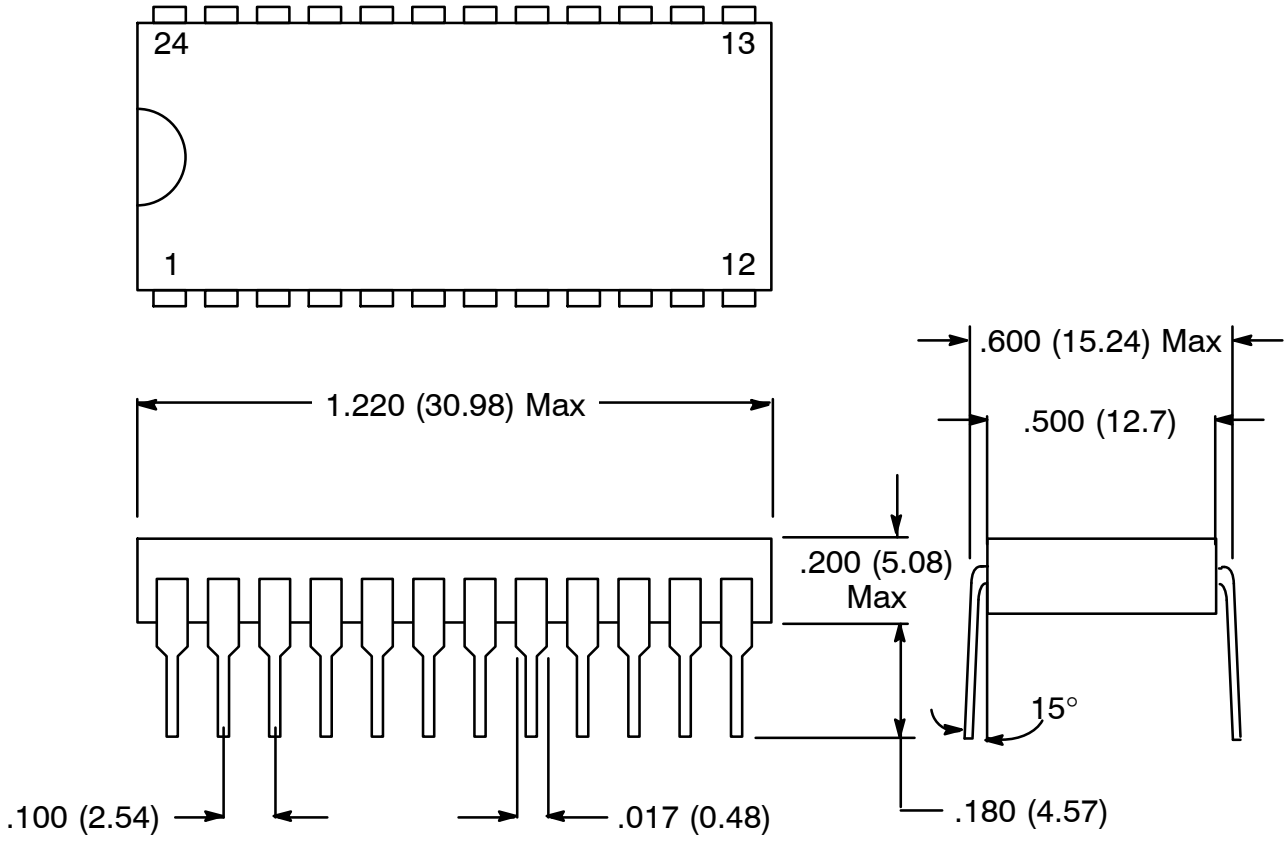
Truth Table

MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latching			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care

Pin Connection Diagram




24
13
1
12
.600 (15.24) Max
1.220 (30.98) Max
.500 (12.7)
.200 (5.08)
Max
15°
.100 (2.54)
.017 (0.48)
.180 (4.57)