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NTE2981 Logic Level MOSFET N-Channel, Enhancement Mode High Speed Switch TO251

Features:

- Dynamic dv/dt Rating
- Repetitive Avalanche rated
- Logic Level Gate Drive
- R_{DS(on)} Specified at V_{GS} = 4V & 5V
- TO251 Type Package

Absolute Maximum Ratings:

| | |
|--|----------------|
| Drain Current, I _D | |
| Continuous (V _{GS} = 5V) | |
| T _C = +25°C | 7.7A |
| T _C = +100°C | 4.9A |
| Pulsed (Note 1) | 31A |
| Total Power Dissipation (T _C = +25°C), P _D | 42W |
| Derate Above 25°C | 0.33W/°C |
| Total Power Dissipation (PC Board Mount, T _C = +25°C, Note 2), P _D | 2.5W |
| Derate Above 25°C | 0.02W/°C |
| Gate-Source Voltage, V _{GS} | ±10V |
| Single Pulsed Avalanche Energy (Note 3), E _{AS} | 210mJ |
| Avalanche Current (Note 1), I _{AR} | 7.7A |
| Repetitive Avalanche Energy (Note 1), E _{AR} | 4.2mJ |
| Peak Diode Recovery dv/dt (Note 4), dv/dt | 5.5V/ns |
| Operating Junction Temperature Range, T _J | -55° to +150°C |
| Storage Temperature Range, T _{stg} | -55° to +150°C |
| Maximum Lead Temperature (During Soldering, 1.6mm from case, 10sec), T _L | +260°C |
| Maximum Thermal Resistance: | |
| Junction-to-Case, R _{thJC} | 3.0°C/W |
| Junction-to-Ambient (PCB Mount, Note 2), R _{thJA} | 50°C/W |
| Junction-to-Ambient, R _{thJA} | 110°C/W |

- Note 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
 Note 2. When mounted on a 1" square PCB (FR-4 or G-10 material).
 Note 3. L = 5.3mH, V_{DD} = 25V, R_G = 25Ω, Starting T_J = +25°C, I_{AS} = 7.7A.
 Note 4. I_{SD} ≤ 9.2A, di/dt ≤ 110A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ +150°C.

Electrical Characteristics: ($T_J = +25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------------------------|---|-----|------|------|--------------------|
| Drain–Source Breakdown Voltage | BV_{DSS} | $V_{GS} = 0V, I_D = 250\mu A$ | 100 | – | – | V |
| Breakdown Voltage Temperature Coefficient | $\Delta V_{(BR)DSS} / \Delta T_J$ | Reference to $+25^\circ\text{C}$, $I_D = 1\text{mA}$ | – | 0.13 | – | $V/^\circ\text{C}$ |
| Static Drain–Source ON Resistance | $R_{DS(on)}$ | $V_{GS} = 5V, I_D = 4.6A$, Note 5 | – | – | 0.27 | Ω |
| | | $V_{GS} = 4V, I_D = 3.9A$, Note 4 | – | – | 0.38 | Ω |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\mu A$ | 1.0 | – | 2.0 | V |
| Forward Transconductance | g_{fs} | $V_{DS} = 50V, I_D = 4.6A$, Note 5 | 4.4 | – | – | mhos |
| Drain–to–Source Leakage Current | I_{DSS} | $V_{DS} = 100V, V_{GS} = 0$ | – | – | 25 | μA |
| | | $V_{DS} = 80V, V_{GS} = 0V, T_C = +125^\circ\text{C}$ | – | – | 250 | μA |
| Gate–Source Leakage Forward | I_{GSS} | $V_{GS} = 10V$ | – | – | 100 | nA |
| Gate–Source Leakage Reverse | I_{GSS} | $V_{GS} = -10V$ | – | – | -100 | nA |
| Total Gate Charge | Q_g | $V_{GS} = 5V, I_D = 9.2A, V_{DS} = 80V$, Note 5 | – | – | 12 | nC |
| Gate–Source Charge | Q_{gs} | | – | – | 3.0 | nC |
| Gate–Drain (“Miller”) Charge | Q_{gd} | | – | – | 7.1 | nC |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{DD} = 50V, I_D = 9.2A, R_G = 9.0\Omega, R_D = 5.2\Omega$, Note 5 | – | 9.8 | – | ns |
| Rise Time | t_r | | – | 64 | – | ns |
| Turn–Off Delay Time | $t_{d(off)}$ | | – | 21 | – | ns |
| Fall Time | t_f | | – | 27 | – | ns |
| Internal Drain Inductance | L_D | Between lead, 6mm (0.25”) from package and center of die contact | – | 4.5 | – | nH |
| Internal Source Inductance | L_S | | – | 7.5 | – | nH |
| Input Capacitance | C_{iss} | $V_{GS} = 0V, V_{DS} = 25V, f = 1\text{MHz}$ | – | 490 | – | pF |
| Output Capacitance | C_{oss} | | – | 150 | – | pF |
| Reverse Transfer Capacitance | C_{rss} | | – | 30 | – | pF |
| Source–Drain Diode Ratings and Characteristics | | | | | | |
| Continuous Source Current | I_S | (Body Diode) | – | – | 7.7 | A |
| Pulse Source Current | I_{SM} | (Body Diode) Note 1 | – | – | 31 | A |
| Diode Forward Voltage | V_{SD} | $T_J = +25^\circ\text{C}, I_S = 7.7A, V_{GS} = 0V$, Note 5 | – | – | 2.5 | V |
| Reverse Recovery Time | t_{rr} | $T_J = +25^\circ\text{C}, I_F = 9.2A, di/dt = 100A/\mu s$, Note 5 | – | 110 | 140 | ns |
| Reverse Recovery Charge | Q_{rr} | | – | 0.8 | 1.0 | μC |
| Forward Turn–On Time | t_{on} | Intrinsic turn–on time is negligible (turn–on is dominated by $L_S + L_D$) | | | | |

Note 1. Repetitive Rating: Pulse width limited by maximum junction temperature.

Note 5. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

