



MX553BBA312M500

Ultra-Low Jitter 312.5MHz LVPECL XO

ClockWorks® FUSION

General Description

The MX553BBA312M500 is an ultra-low phase jitter XO with LVPECL output optimized for high line rate applications.

Applications

- 10/40/400 Gigabit Ethernet
- Fibre Channel 10G/12G SERDES

Absolute Maximum Ratings

Supply Voltage (VIN)	+3.6V
Lead Temperature (soldering, 10s)	260°C
Storage Temperature (T _s)	125°C
ESD Rating (HBM)	2kV

Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 50 Ohms to VDD - 2V.¹

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				120	mA
F0	Center Frequency			312.5		MHz
	Frequency Stability	Note 2			±50	ppm
∅j	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		155 108	200 -	fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		85		350	ps
	Duty Cycle		45		55	%
VOH	Output High Voltage	LVPECL output levels	VDD - 1.35	VDD - 1.01	VDD - 0.8	V
VOL	Output Low Voltage	LVPECL output levels	VDD - 2.0	VDD - 1.78	VDD - 1.6	V
Vswing	Peak to Peak Output Voltage Swing		0.65	0.77	0.95	V

Notes:

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax + 1 (408) 474-1000 • <http://www.micrel.com>

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Revision 1.0
tcghelp@micrel.com or (408) 955-1690

Features

- 312.5MHz LVPECL
- Typical phase noise:
 - 108fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 5mm x 3.2mm LGA package

Operating Ratings

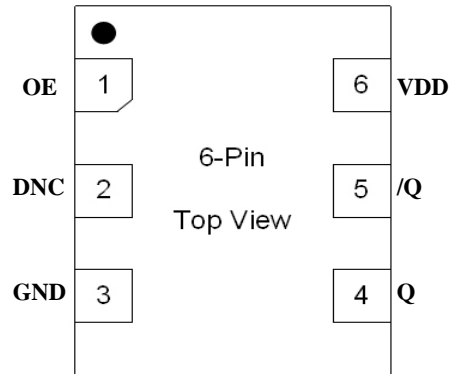
Supply Voltage (VIN)	+2.375V to +3.63V
Ambient Temperature (TA)	-40°C to +85°C

Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX553BBA312M500	MX553B	BA3125	Tube	6-Pin 5mm x 3.2mm LGA
MX553BBA312M500 TR	MX553B	BA3125	Tape and Reel	6-Pin 5mm x 3.2mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVPECL	Clock Output Frequency = 312.5MHz
6	VDD	PWR		Power Supply

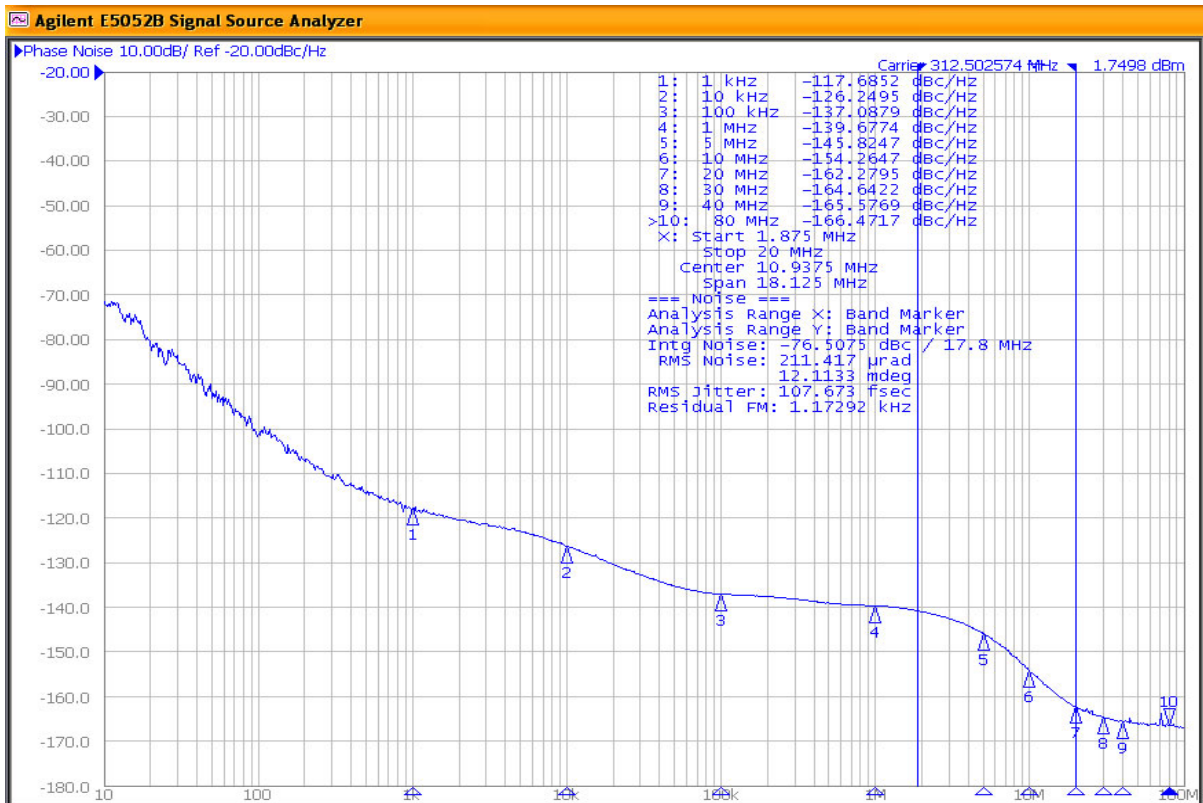


Figure 1. LVPECL Output 312.5MHz 1.875MHz-20MHz 108fs

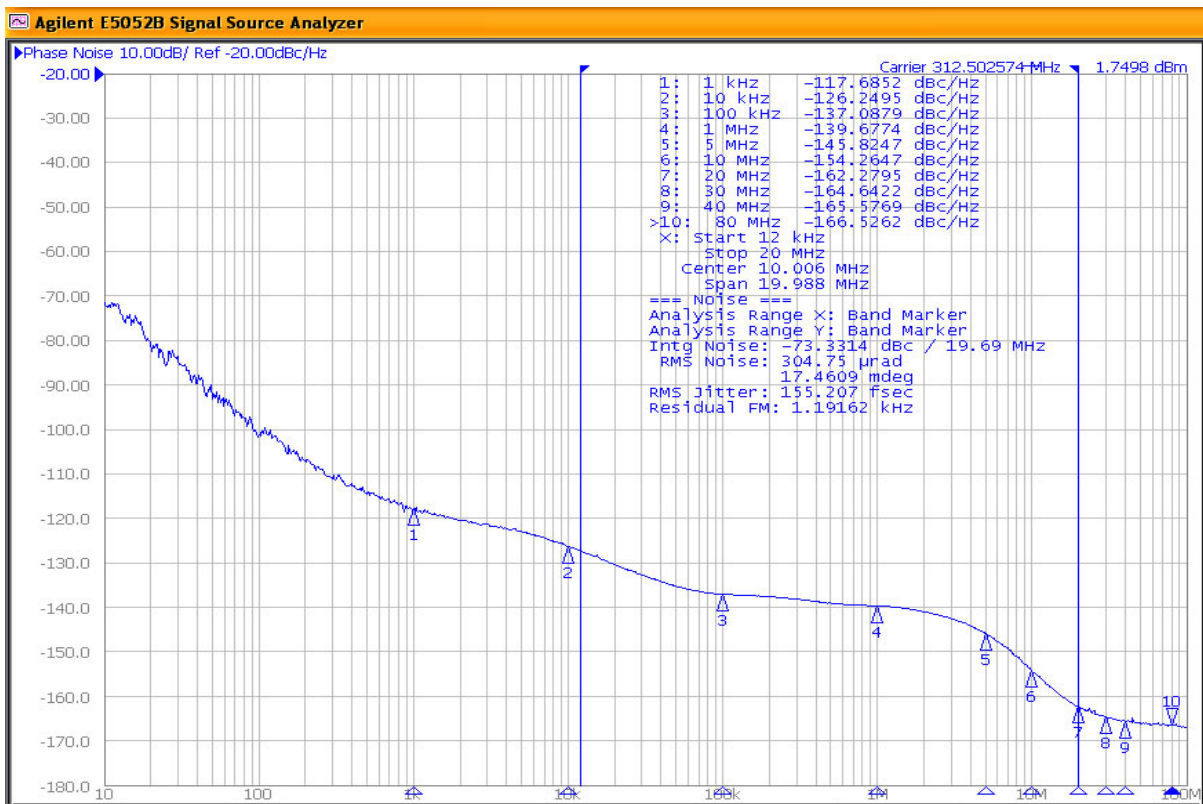
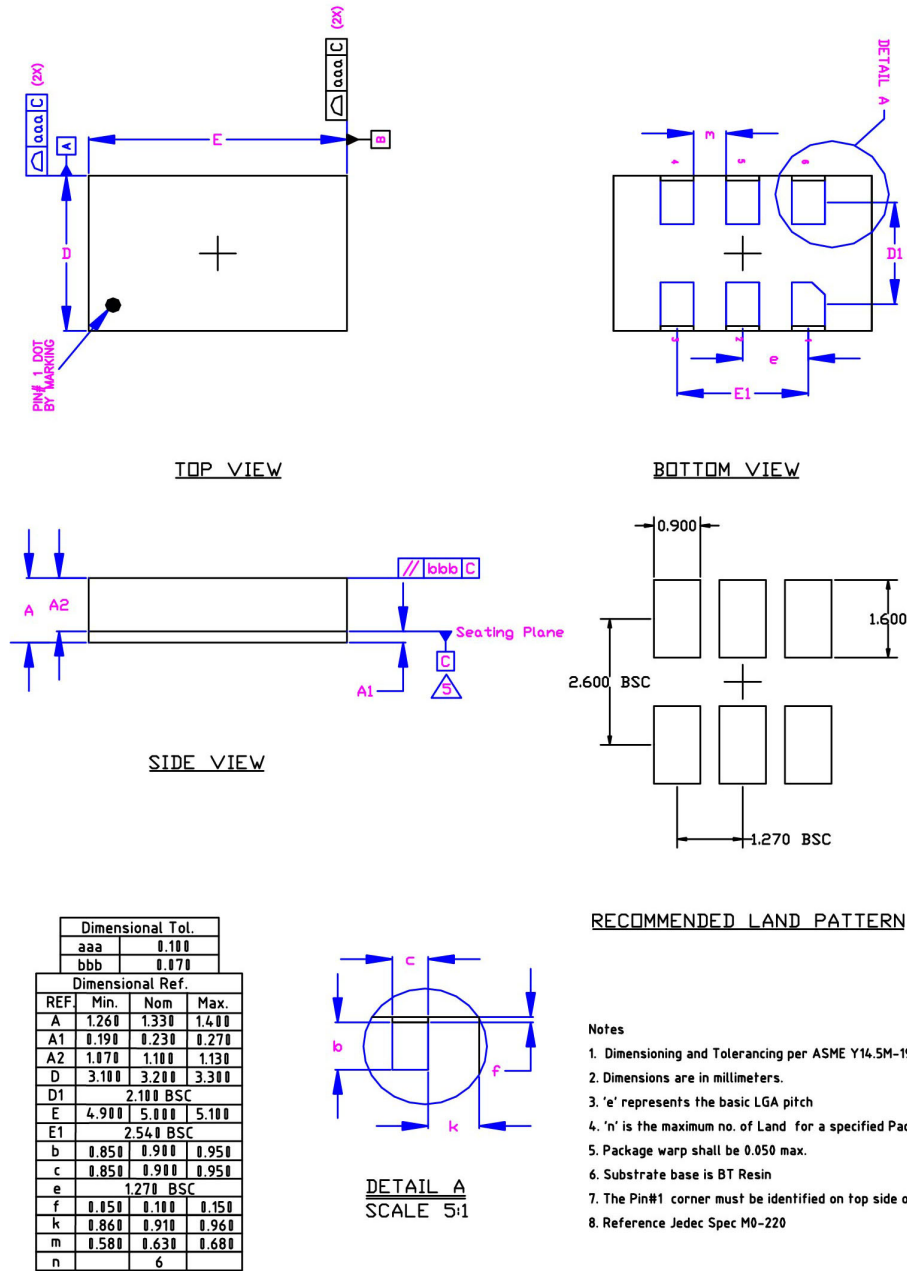


Figure 2. LVPECL Output 312.5MHz 12kHz-20MHz 155fs

Package Information and Recommended Land Pattern for 6-Pin LGA³



RECOMMENDED LAND PATTERN

- Notes**
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
 2. Dimensions are in millimeters.
 3. 'e' represents the basic LGA pitch
 4. 'n' is the maximum no. of Land for a specified Package.
 5. Package warp shall be 0.050 max.
 6. Substrate base is BT Resin
 7. The Pin#1 corner must be identified on top side only.
 8. Reference Jecid Spec M0-220

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
 TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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