Atmel SAM D21EL / SAM D21GL

SMART ARM-Based Microcontroller

DATASHEET SUMMARY

Description

The Atmel® | SMART™ SAM D21L is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor. The SAM D21L devices are offered in 32- and 48-pins packages with up 64KB Flash and 8KB of SRAM and are designed to operate at a maximum frequency of 48MHz and reach 2.46 Coremark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The Atmel SAM D21L devices provide the following features: In-system programmable Flash, twelve-channel direct memory access (DMA) controller, 12 channel Event System, programmable interrupt controller, up to 38 programmable I/O pins, 32-bit real-time clock and calendar, up to five 16-bit Timer/Counters (TC) and three 24-bit Timer/Counters for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications. The series provide up to five Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I^2C up to 3.4MHz, SMBus, PMBus, and LIN slave; up to eighteen-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, four analog comparators with window mode, programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM D21L devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM D21L devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

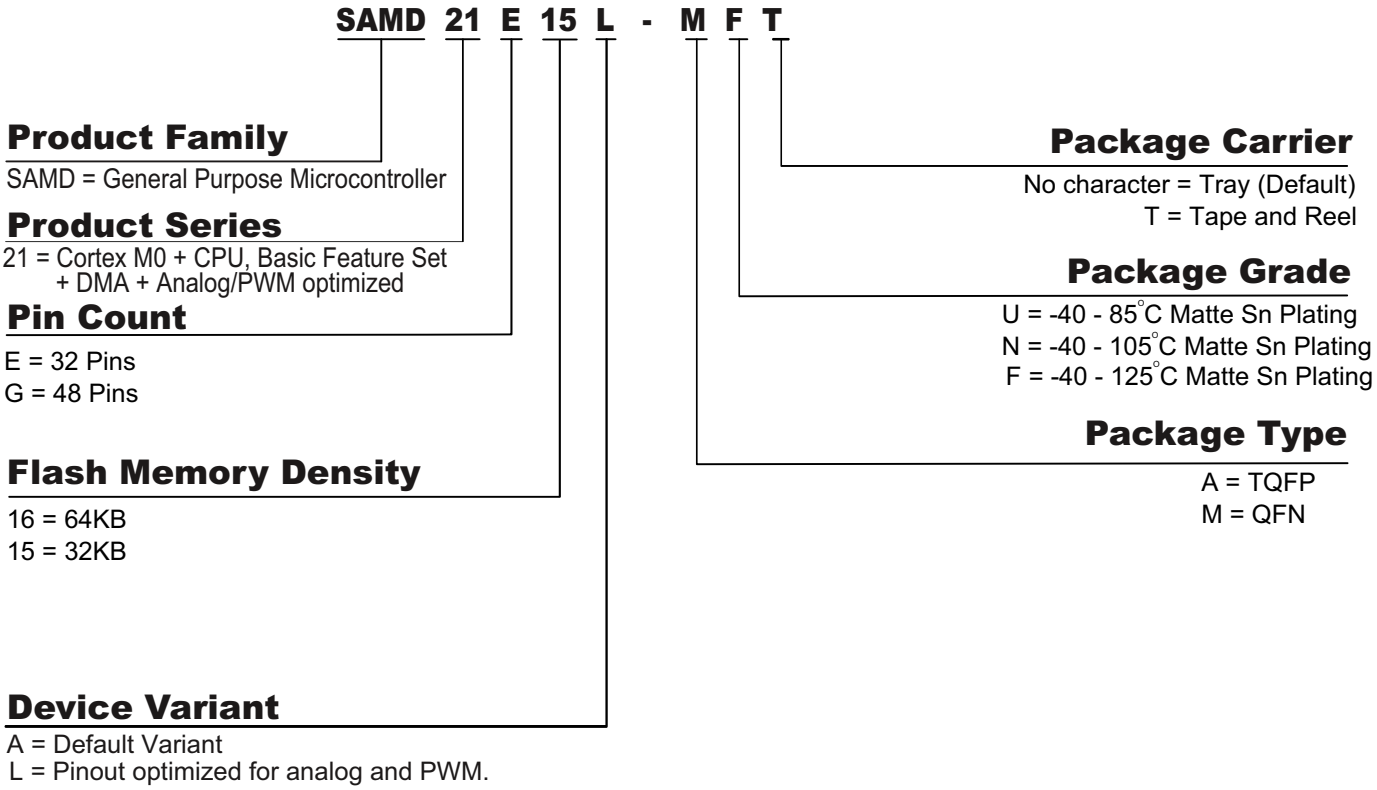
Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
    - Single-cycle hardware multiplier
    - Micro Trace Buffer (MTB)
- Memories
  - 32/64KB in-system self-programmable Flash
  - 4/8KB SRAM Memory
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz Digital Frequency Locked Loop (DFLL48M) and 48MHz to 96MHz Fractional Digital Phase Locked Loop (FDPLL96M)
  - External Interrupt Controller (EIC)
  - 16 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle and standby sleep modes
  - SleepWalking peripherals
- Peripherals
  - 12-channel Direct Memory Access Controller (DMAC)
  - 12-channel Event System
  - Up to five 16-bit Timer/Counters (TC), configurable as either:
    - One 16-bit TC with compare/capture channels
    - One 8-bit TC with compare/capture channels
    - One 32-bit TC with compare/capture channels, by using two TCs
  - Three 24-bit Timer/Counters for Control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - Up to five Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - I^2C up to 3.4MHz
    - SPI
    - LIN slave
  - One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 18 channels
    - Differential and single-ended input
    - 1/2x to 16x programmable gain stage
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - 10-bit, 350ksps Digital-to-Analog Converter (DAC)
  - Four Analog Comparators (AC) with window compare function
- I/O
  - Up to 38 programmable I/O pins
- Packages
  - 32-pin TQFP, QFN
  - 48-pin QFN
- Operating Voltage
  - 1.62V – 3.63V

1. Configuration Summary

	SAM D21ExL	SAM D21GxL
Pins	32	48
General Purpose I/O-pins (GPIOs)	26	38
Flash	64/32KB	64KB
SRAM	8/4KB	8KB
Timer Counter (TC) instances	3	5
Waveform output channels per TC instance	2	2
Timer Counter for Control (TCC) instances	3	3
Waveform output channels per TCC	8/4/2	8/4/2
DMA channels	12	12
Serial Communication Interface (SERCOM) instances	5	5
Analog-to-Digital Converter (ADC) channels	14	18
Analog Comparators (AC)	4	4
Digital-to-Analog Converter (DAC) channels	1	1
Real-Time Counter (RTC)	Yes	Yes
RTC alarms	1	1
RTC compare values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values
External Interrupt lines	16	16
Maximum CPU frequency	48MHz	
Packages	QFN TQFP	QFN
Oscillators	0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32kHz ultra-low-power internal oscillator (OSCULP32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M) 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)	
Event System channels	12	12
SW Debug Interface	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes

2. Ordering Information



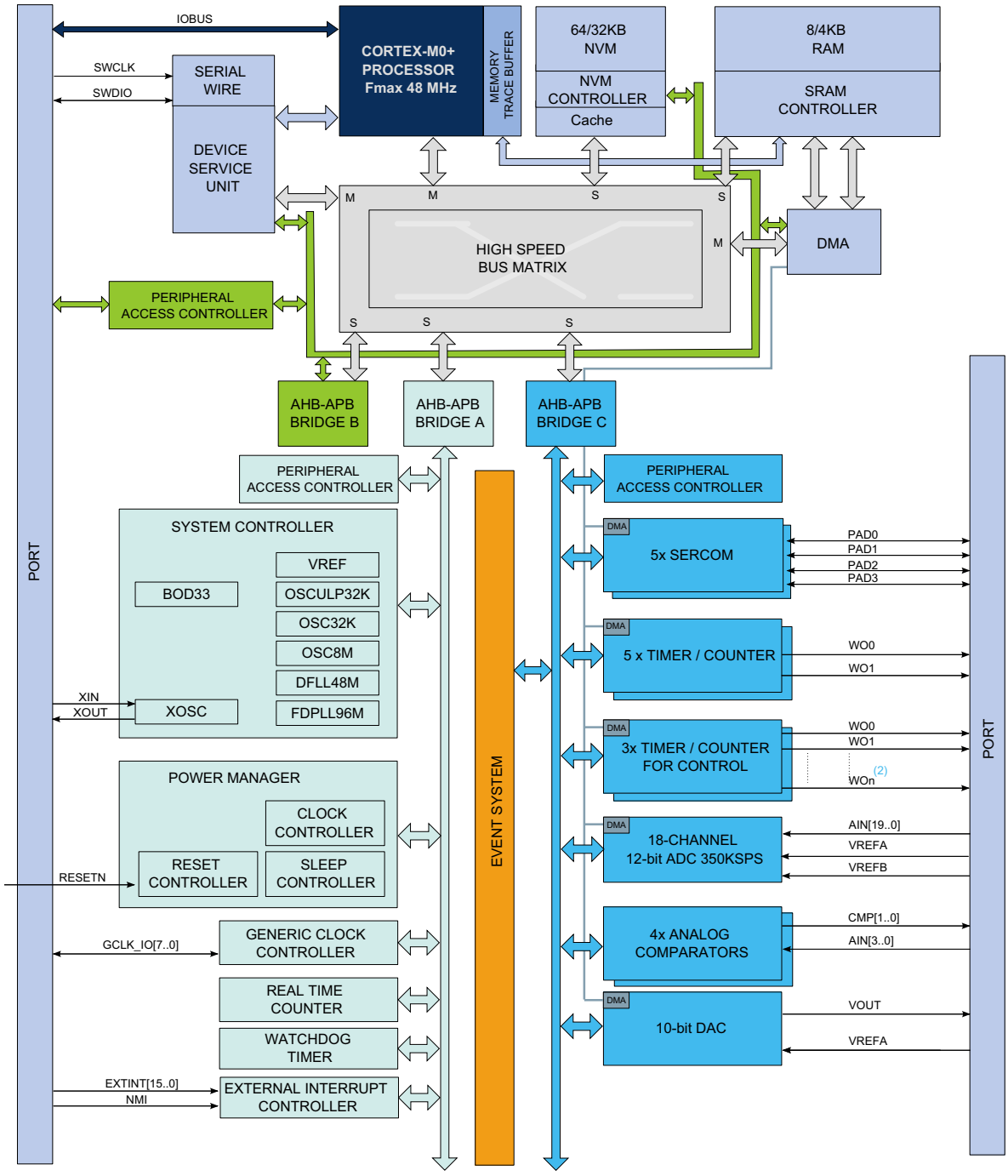
2.1 SAM D21ExL

Ordering Code	FLASH (bytes)	SRAM (bytes)	Temp.Range	Package	Carrier Type
ATSAMD21E15L-MNT	32K	4K	105°C	QFN32	Tape & Reel
ATSAMD21E16L-MNT	64K	8K			
ATSAMD21E15L-AFT	32K	4K	125°C	TQFP32	Tape & Reel
ATSAMD21E15L-MFT				QFN32	
ATSAMD21E16L-AFT	64K	8K	125°C	TQFP32	Tape & Reel
ATSAMD21E16L-MFT				QFN32	

2.2 SAM D21GxL

Ordering Code	FLASH (bytes)	SRAM (bytes)	Temp.Range	Package	Carrier Type
ATSAMD21G16L-MUT	64K	8K	85°C	QFN48	Tape & Reel
ATSAMD21G16L-MNT	64K	8K	105°C	QFN48	Tape & Reel

3. Block Diagram

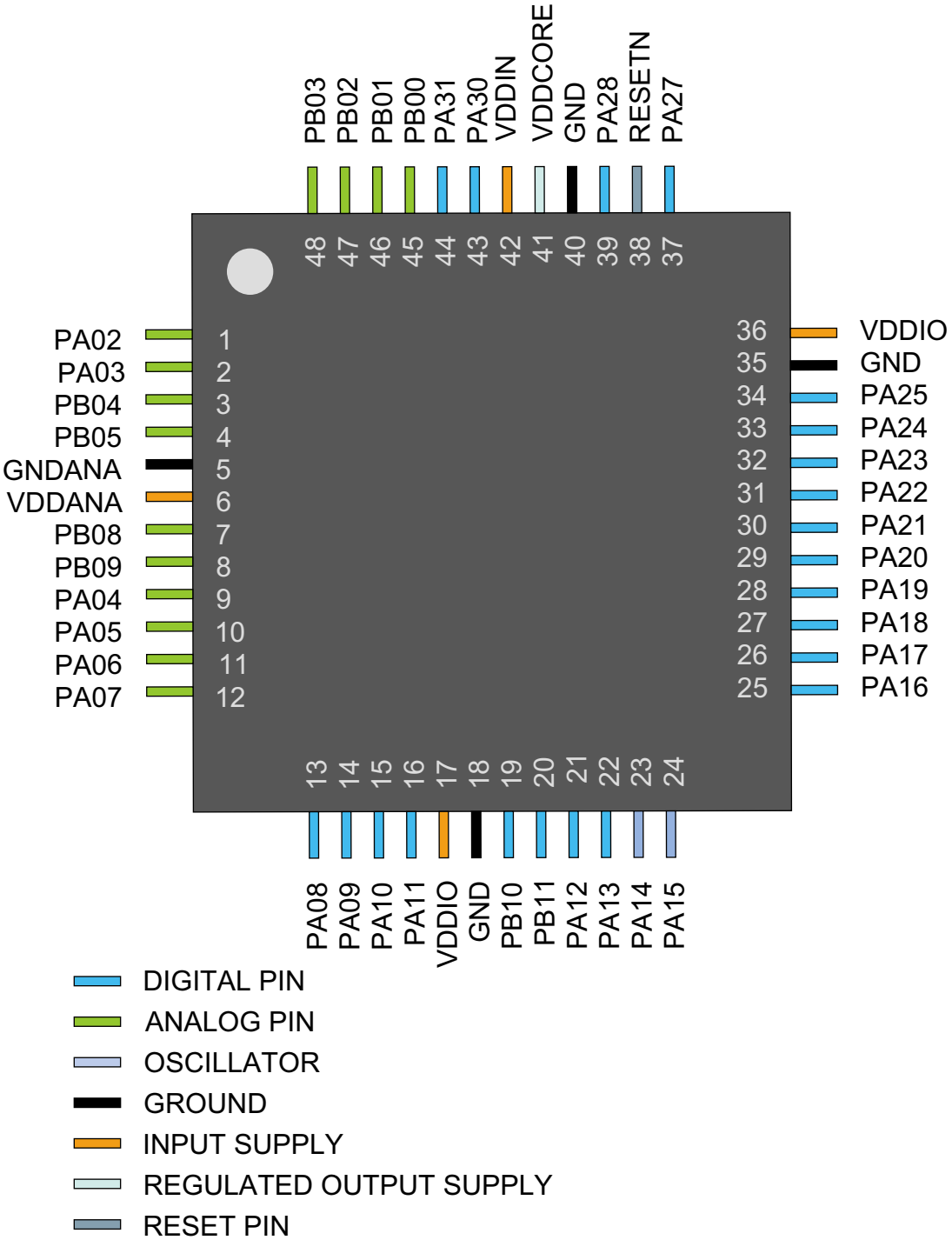


1. Some products have different number of SERCOM instances, Timer/Counter instances and ADC signals.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines.

4. Pinout

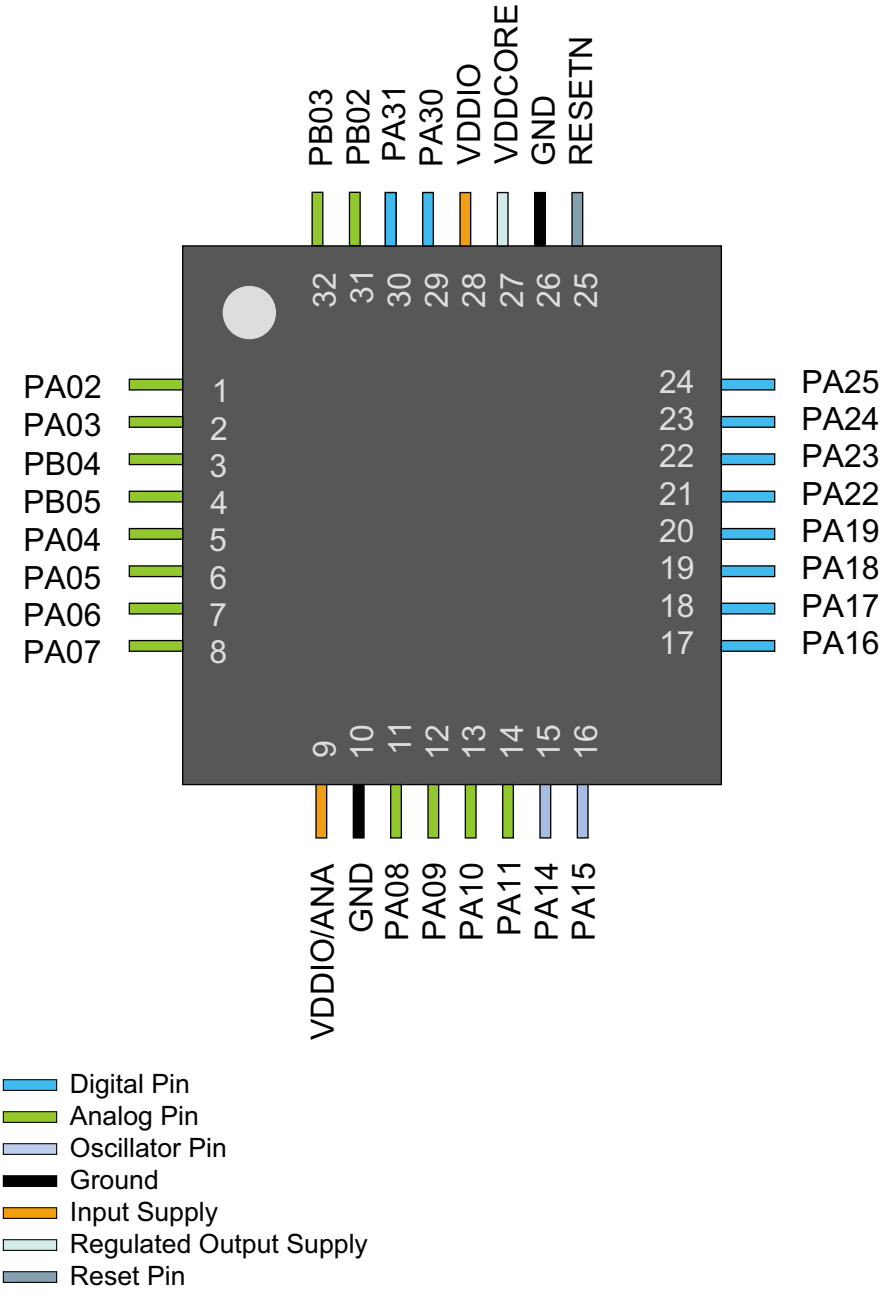
4.1 SAM D21GxL

4.1.1 QFN48



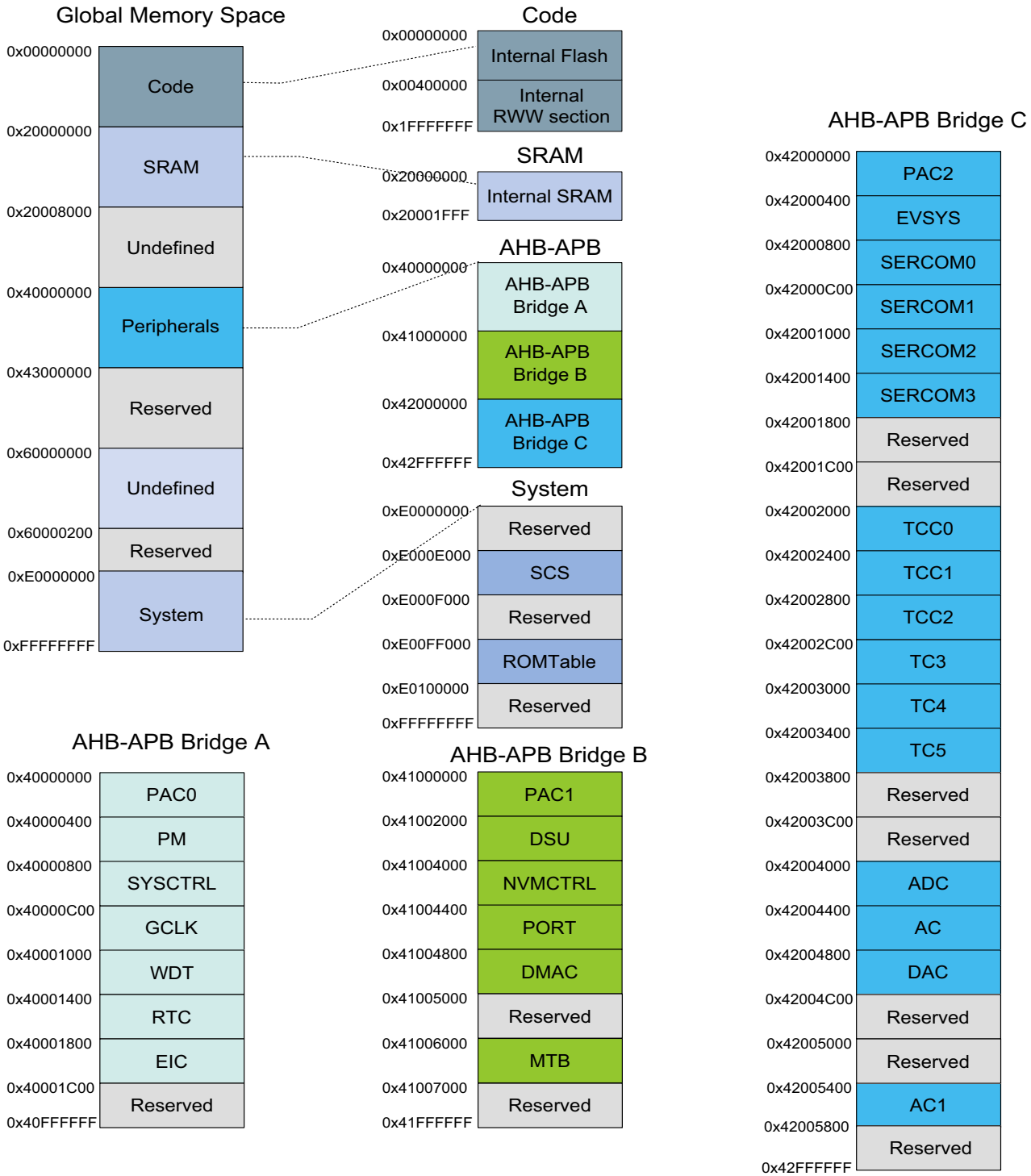
4.2 SAM D21ExL

4.2.1 QFN32 / TQFP32



5. Product Mapping

Figure 5-1. Atmel | SMART SAM D21L Product Mapping



This figure represents the full configuration of the Atmel® SAM D21 with maximum flash and SRAM capabilities and a full set of peripherals. Refer to the "Configuration Summary" on page 3 for details.

6. Processor And Architecture

6.1 Cortex M0+ Processor

The Atmel | SMART SAM D21L implements the ARM® Cortex™-M0+ processor, which is based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 processor, and upward compatible to Cortex-M3 and M4 processors.

For more information refer to www.arm.com.

6.1.1 Cortex M0+ Configuration

Features	Configuration option	Atmel | SMART SAM D21L configuration
Interrupts	External interrupts 0-32	32
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Absent(1)
Memory Protection Unit	Not present or 8-region	Not present
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

Note: 1. All software run in privileged mode only

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA®-3 AHB-Lite™ system interface that provides connections to peripherals and all system memory, including flash and RAM
- Single 32-bit I/O port bus interfacing to the PORT with one-cycle loads and stores

7. Packaging Information

7.1 Thermal Considerations

7.1.1 Thermal Resistance Data

Table 7-1 summarizes the thermal resistance data depending on the package.

Table 7-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
32-pin TQFP	64.7 °C/W	23.1 °C/W
32-pin QFN	40.9 °C/W	15.2 °C/W
48-pin QFN	32.0°C/W	10.9 °C/W

7.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

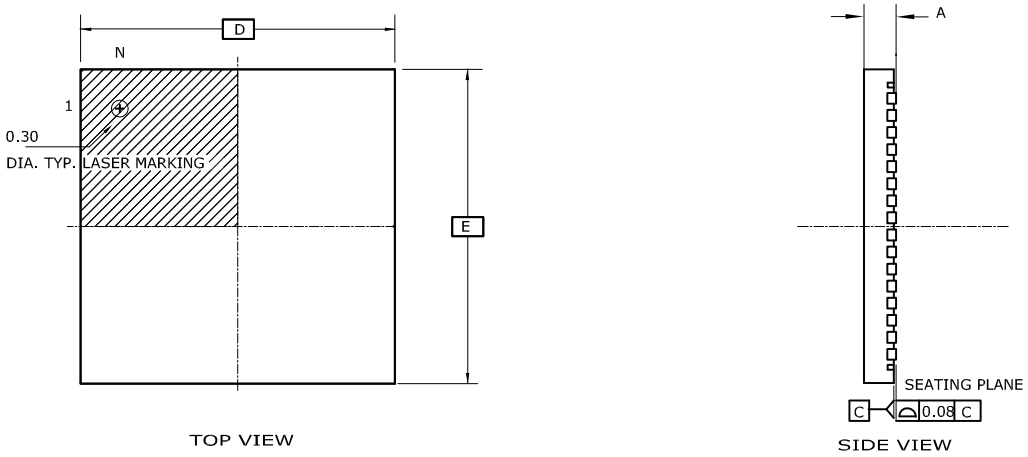
- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 7-1.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 7-1.
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W).
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

7.2 Package Drawings

7.2.1 48-pin QFN

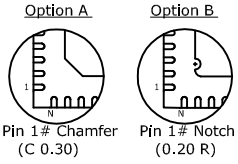
DRAWINGS NOT SCALED



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
D/E		7.00 BSC		
D2/E2	5.05	5.15	5.25	
b	0.18	0.25	0.30	
e		0.50 BSC		
L	0.30	0.40	0.50	
N		48		



Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

Table 7-2. Device and Package Maximum Weight

140	mg

Table 7-3. Package Characteristics

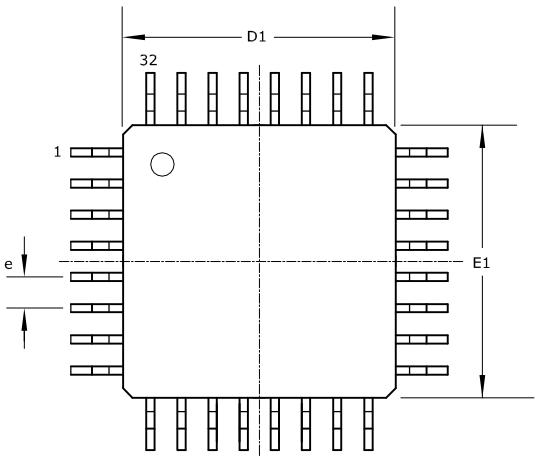
Moisture Sensitivity Level	MSL3

Table 7-4. Package Reference

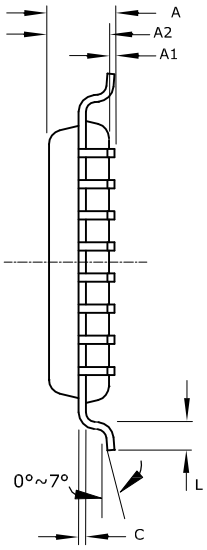
JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

7.2.2 32-pin TQFP

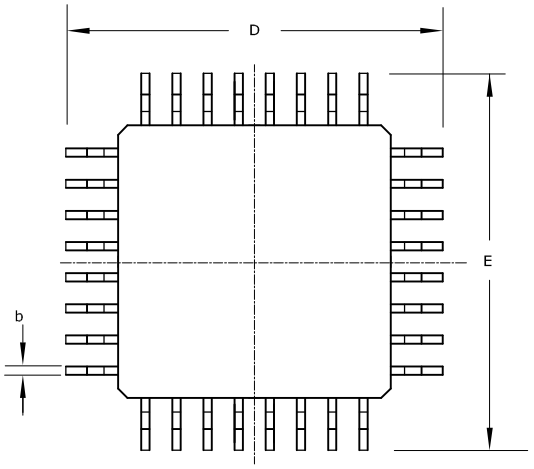
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	1.00	1.05	
D/E	8.75	9.00	9.25	
D1/E1	6.90	7.00	7.10	2
C	0.09	-----	0.20	
L	0.45	-----	0.75	
b	0.30	-----	0.45	
e	0.80 TYP			
n	32			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

Table 7-5. Device and Package Maximum Weight

100	mg

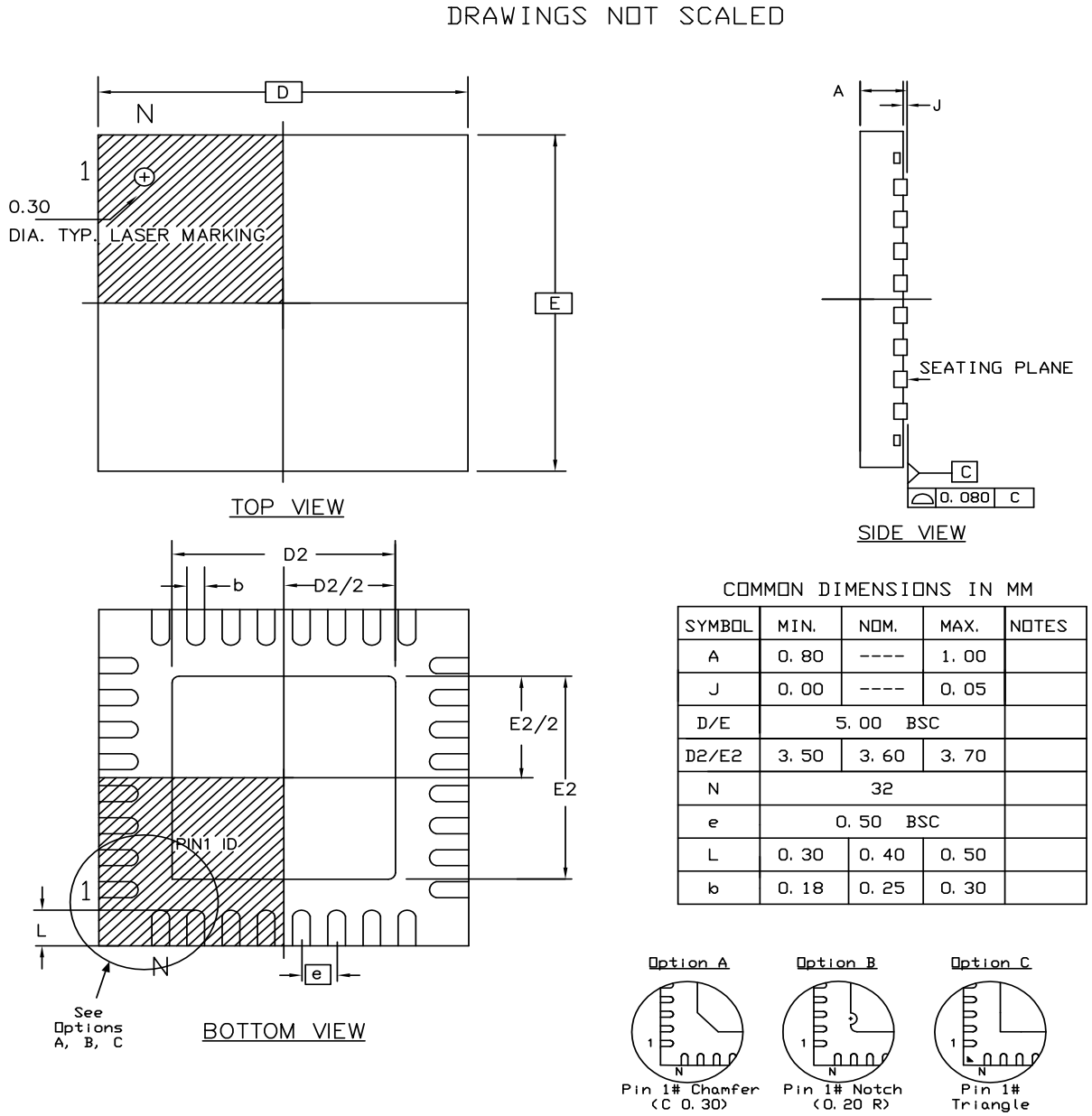
Table 7-6. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 7-7. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

7.2.3 32-pin QFN



SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	----	1.00	
J	0.00	----	0.05	
D/E		5.00 BSC		
D2/E2	3.50	3.60	3.70	
N		32		
e		0.50 BSC		
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	

Table 7-8. Device and Package Maximum Weight

90	mg

Table 7-9. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 7-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

7.3 Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max
Preheat Temperature 175°C +/-25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

A maximum of three reflow passes is allowed per component.

Table of Contents

Atmel | Enabling Unlimited Possibilities®

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**